Sequential Symbol Synchronizers based on Pulse Comparation by Positive Transitions at Quarter Rate

Antonio D. Reis^{1,2}, Jose F. Rocha¹, Atilio S. Gameiro¹ and Jose P. Carvalho²

Abstract - This work presents the synchronizer based on pulse comparation, between variable and fixed pulses.

This synchronizer has two variants, one operating by both transitions at the bit rate and other operating by positive transitions at quarter rate. Each variant has two versions namely the manual and the automatic.

The objective is to study the four synchronizers and evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal Noise Ratio).

Keywords - Synchronism in Digital Communications

I. INTRODUCTION

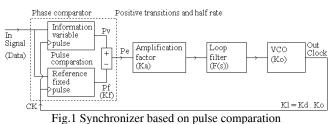
This work studies the sequential symbol synchronizer, with a phase comparator based on a pulse comparation, between a variable pulse Pv and a fixed reference pulse Pf.

The synchronizer has four types supported in two variants one operating by both transitions at the bit rate and other operating by positive transitions at quarter rate [1, 2, 3, 4, 5].

The variant at the rate has two versions namely the manual (b-m) and automatic (b-a). The variant at quarter rate has two versions namely the manual (p-m/4) and automatic (p-a/4).

The difference between them is in the phase comparator since the other blocks are equal [6, 7, 8, 9, 10, 11, 12].

The error pulse Pe (Pv - Pf) controls the VCO (Voltage Controlled Oscillator) to synchronize with the input data. The VCO output is the clock, with good quality, that samples appropriately the input data and retimes its bit duration. Fig.1 shows the blocks of the symbol synchronizer.



Kf is the phase comparator gain, F(s) is the loop filter, Ko is the VCO gain and Ka is the loop gain factor that controls the root locus and then the loop characteristics.

In priori and actual-art state was developed various synchronizers, now is necessary to know their performance.

The motivation of this work is to create new synchronizers

¹Antonio D. Reis, Jose F. Rocha and Atilio S. Gameiro are with Dep. Electrónica, Universidade Aveiro / Instituto Telecomunicações, 3800 Aveiro, Portugal, E-mail: amg@det.ua.pt; frocha@det.ua.pt.

²Antonio D. Reis and Jose P. Carvalho are with the Dep. Fisica, Universidade da Beira Interior Covilhã / Unidade Detecção Remota, 6200 Covilhã, Portugal, E-mail: adreis@ubi.pt; pacheco@ubi.pt.

and to evaluate their performance with noise. This contribution increases the knowledge about synchronizers.

Following, we present the variant both transitions at rate with their manual (b-m) and automatic (b-a) versions. Next, we present the variant positive transitions at quarter rate with their manual (p-m/4) and automatic (p-a/4) versions.

After, we present the design and tests. Then, we present the results. Finally, we present the conclusions.

II. SYNCHRONIZERS OPERATING AT THE RATE

The synchronizer with its phase comparator operates, here, by both transitions at the data transmission rate.

This variant has the manual (b-m) and automatic (b-a) versions, the difference is in phase comparator. The variable pulse Pv, produced by the first flip flop with exor, is equal in the two versions, but the fixed pulse Pf is different [1, 2].

A. Both transitions, at the rate and manual

The manual version has a phase comparator, where the fixed pulse Pf is produced by an exor with a delay $\Delta t=T/2$, that needs a previous manual adjustment (Fig.2)

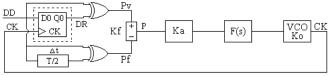
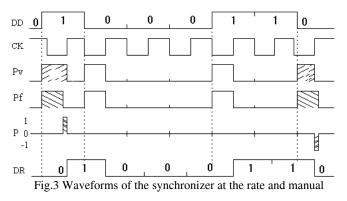


Fig.2 Synchronizer both at the rate and manual (b-m)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig.3 shows the waveforms of the synchronizer operating at the rate and manual version.



The error pulse Pe diminishes and disappear at the equilibrium point.

B. Both transitions, at the rate and automatic

The automatic version has a phase comparator where the fixed pulse Pf is produced automatically by the second flip flop with exor, without previous adjustment (Fig.4).

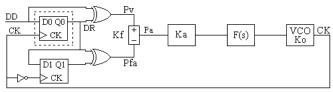
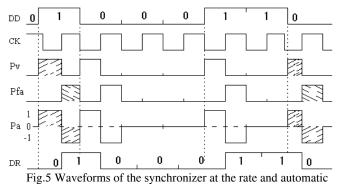


Fig.4 Synchronizer both at the rate and automatic (b-a)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig.5 shows the waveforms of the synchronizer operating at the rate and automatic version.



The error pulse Pe don't disappear, but the variable area Pv is equal to the fixed one Pf at the equilibrium point.

III. SYNCHRONIZERS OPERATING AT QUARTER

RATE

The synchronizer with its phase comparator operates, here, by positive transitions at quarter data transmission rate.

This variant has the manual (p-m/4) and the automatic (p-a/4) versions, the difference is only in the phase comparator. The variable pulse Pvp, based in the four first flip flops with multiplexer, is equal in the two versions, but the fixed pulse Pfp is produced from a different way [3, 4].

A. Positive transitions, at quarter rate and manual

The manual version has a phase comparator, where the fixed pulse Pf is produced by an exor with a delay $\Delta t=T/2$, that needs a previous manual adjustment (Fig.6).

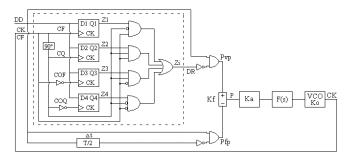
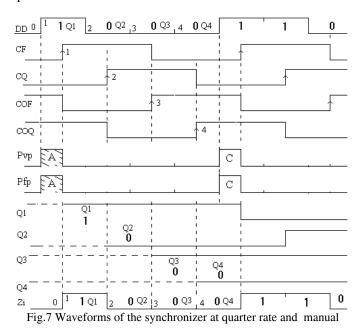


Fig.6 Synchronizer positive at quarter rate and manual (p-m/4) The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig.7 shows the waveforms of the synchronizer operating at quarter rate and manual version.



The error pulse Pe diminishes and disappear at the equilibrium point

B. Positive transitions, quarter rate and automatic

The automatic version has a phase comparator, where the fixed pulse Pf is produced automatically by the seconds flip flops and multiplexer with exor, without previous adjustment (Fig.8).

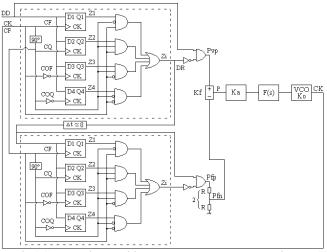
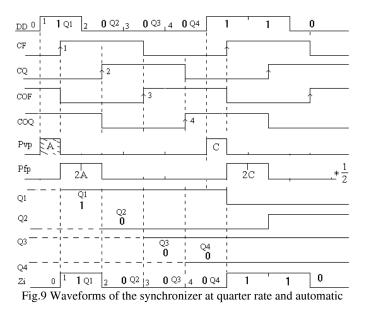


Fig.8 Synchronizer positive at quarter rate and automatic (p-a/4)

The variable pulse Pv minus the fixed pulse Pf (Pv-Pf) determines the error phase that controls the VCO.

Fig.9 shows the waveforms of the synchronizer at quarter rate and automatic version.



The error pulse Pe don't disappear but the positive area is equal to the negative at the equilibrium point.

IV. DESIGN, TESTS AND RESULTS

We will present the design, the tests and the results of the referred synchronizers [5].

A. Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is Kl=Kd.Ko=Ka.Kf.Ko where Kf is the phase comparator gain, Ko is the VCO gain and Ka is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate tx=1baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is fCK=1Hz.

We choose a normalized external noise bandwidth Bn = 5Hz and a normalized loop noise bandwidth Bl = 0.02Hz. Later, we can disnormalize these values to the appropriated transmission rate tx.

Now, we will apply a signal with noise ratio SNR given by the signal amplitude Aef, noise spectral density No and external noise bandwidth Bn, so the SNR = A_{ef}^2 (No.Bn). But, No can be related with the noise variance σn and inverse sampling $\Delta \tau = 1/Samp$, then No= $2\sigma n^2 \Delta \tau$, so SNR= A_{ef}^2 ($2\sigma n^2 \Delta \tau Bn$) = $0.5^2/(2\sigma n^{2*} 10^{-3*} 5)$ = $25/\sigma n^2$.

After, we observe the output jitter UI as function of the input signal with noise SNR. The dimension of the loops is

- 1st order loop:

The loop filter F(s)=1 with cutoff frequency 0.5Hz (Bp=0.5 Hz is 25 times bigger than Bl=0.02Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{KdKoF(s)}{s + KdKoF(s)} = \frac{KdKo}{s + KdKo}$$
(1)

the loop noise bandwidth is

$$BI = \frac{KdKo}{4} = Ka \frac{KfKo}{4} = 0.02Hz$$
(2)

Then, for the analog synchronizers, the loop bandwidth is Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=1/2; Ko=2 π) (*Ka.Km.A.B.Ko*)/4 = 0.02 -> $Ka=0.08*2/\pi$ (3)

For the hybrid synchronizers, the loop bandwidth is Bl=0.02=(Ka.Kf.Ko)/4 with (Km=1, A=1/2, B=0.45; Ko=2\pi) (Ka.Km.A.B.Ko)/4 = 0.02 -> Ka=0.08*2.2/\pi (4)

For the combinational synchronizers, the loop bandwidth is Bl=0.02=(Ka.Kf.Ko)/4 with $(Kf=1/\pi; Ko=2\pi)$ $(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04$ (5) For the sequential synchronizers, the loop bandwidth is Bl=0.02=(Ka.Kf.Ko)/4 with $(Kf=1/2\pi; Ko=2\pi)$ $(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08$ (6)

The jitter depends on the RMS signal Aef, on the power spectral density No and on the loop noise bandwidth Bl. For analog PLL the jitter is

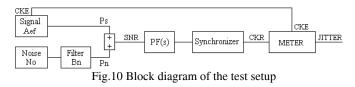
 $\sigma \phi^2 = Bl.No/Aef^2 = Bl.2.\sigma n^2 \Delta \tau = 0.02 \times 10^{-3} \times 2\sigma n^2 / 0.5^2 = 16 \times 10^{-5} .\sigma n^2$ For the others PLLs the jitter formula is more complicated.

- 2^{nd} order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

B. Tests

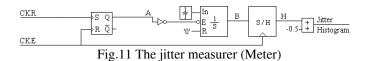
The following figure (Fig.10) shows the setup that was used to test the various synchronizers.



The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

C. Jitter measurer (Meter)

The jitter measurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

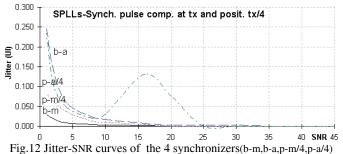


The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram. Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

D. Results

We will present the results (graphics of output jitter UIRMS - input SNR) for the four symbol synchronizers.

Fig.12 shows the jitter-SNR curves of the four synchronizers namely both transitions at rate manual (b-m), both transitions at rate automatic (b-a), positive transitions at quarter rate manual (p-m/4) and positive transitions at quarter rate automatic (p-a/4).



We see that, in general, the output jitter UIRMS decreases gradually with the input SNR increasing. However, the positive quarter rate automatic (p-a/4) has some irregularities.

For high SNR, the four synchronizer jitter curves tend to be similar. However, for low SNR, the manual versions (b-m, p-m/4) are significantly better than the automatic versions (b-a, p-a/4), the both transitions at rate manual (b-m) is slightly the best. Also, for an intermediate SNR (SNR \cong 16), the positive transitions quarter rate automatic (p-a/4) has a very significant jitter perturbation, due to some losses of synchronism.

V. CONCLUSIONS

We studied four synchronizers with one variant operating by both transitions at the rate that has two versions namely the manual (b-m) and automatic (b-a) and other variant operating by positive transitions at quarter rate that has two versions namely the manual (p-m/4) and automatic (p-a/4). Then, we tested their jitter - noise curves.

We observed that, in general, the output jitter curves decreases gradually with the input SNR increasing. However, the positive quarter automatic (p-a/4) has some irregularities.

We verified that, for high SNR, the four synchronizers jitter curves tend to be similar, this is comprehensible since all the synchronizers are digital and have similar noise margin. However, for low SNR, the manual versions (b-m, p-m/4) are significantly better than the automatic versions (b-a, p-a/4), this is comprehensible since the automatic versions have more digital states, then the error state propagation is aggravated. The version both transitions at rate manual (b-m) is slightly the best because has less digital states. Also, for an intermediate SNR (SNR \cong 16) the positive transitions at quarter rate automatic (p-a/4) has a very significant jitter perturbation due to some losses of synchronism.

In the future, we are planning to extend the present study to other types of synchronizers.

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REFERENCES

- [1] J. C. Imbeaux, "performance of the delay-line multiplier circuit for clock and carrier synchronization", IEEE Jou. on Selected Areas in Communications p.82 Jan. 1983.
- [2] Werner Rosenkranz, "Phase Locked Loops with limiter phase detectors in the presence of noise", IEEE Trans. on Communications com-30 N°10 pp.2297-2304. Oct 1982.
- [3] H. H. Witte, "A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrat. Output Signal", Electronics Letters, Vol.19, Is.21, pp.897-898, Oct 1983.
- [4] Charles R. Hogge, "A Self Correcting Clock Recovery Circuit", IEEE Tran. Electron Devices p.2704 Dec 1985.
- [5] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "A New Technique to Measure the Jitter", Proc. III Conf. on Telecommunications pp.64-67 FFoz-PT 23-24 Apr 2001.
- [6] Marvin K. Simon, William C. Lindsey, "Tracking Performance of Symbol Synchronizers for Manchester Coded Data", IEEE Transactions on Communications Vol. com-2.5 N°4, pp.393-408, April 1977.
- [7] J. Carruthers, D. Falconer, H. Sandler, L. Strawczynski, "Bit Synchronization in the Presence of Co-Channel Interference", Proc. Conf. on Electrical and Computer Engineering pp.4.1.1-4.1.7, Ottawa-CA 3-6 Sep. 1990.
- [8] Johannes Huber, W. Liu "Data-Aided Synchronization of Coherent CPM-Receivers" IEEE Transactions on Communications Vol.40 N°1, pp.178-189, Jan. 1992.
- [9] Antonio D'Amico, A. D'Andrea, Reggianni, "Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR", IEEE Jou. on Sattelite Areas in Comm. Vol.19 N°12 pp.2320-2330, Dec. 2001.
- [10] Rostislav Dobkin, Ran Ginosar, Christos P. Sotiriou "Data Synchronization Issues in GALS SoCs", Proc. 10th International Symposium on Asynchronous Circuits and Systems, pp.CD-Ed., Crete-Greece 19-23 Apr. 2004.
- [11] N. Noels, H. Steendam, M. Moeneclaey, "Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers", Proc. IEEE Int Conf. on Comm.(ICC'06) pp.2946-2951, Ist.-TK, 11-15 Jun 2006.
- [12] A. D. Reis, J. F. Rocha, A. S. Gameiro, J. P. Carvalho "Effects of the Prefilter Type on Digital Symbol Synchronizers", Proc. VII Symposium on Enabling Optical Network and Sensors (SEONs 2009) pp.35-36, Lisboa (Amadora)-PT 26-26 June 2009.