Generator of Synchronizing Digital Signals with Microcontroller PIC18F252

Tsanko V. Karadzhov[1] and Ivelina S. Balabanova[2]

***Abstract* – Synchronizing signal generators are an integral part of the synchronous digital devices. This makes it necessary to develop new methods and principles in the design of such generators. Deficiencies in the classical schemes are synchronizing signal delays in logic elements that can lead to incorrect output responses. This paper presents the design of a generator for digital synchronizing signal microcontroller PIC18F252, in which the parameters of the output signals have been improved.**

***Keywords* – Microcontroller, Digital signals, Generator.**

I. INTRODUCTION

This paper presents a circuit for producing dephased pulses with CMOS logical elements, a rectangular pulse generator voltage and a frequency divider, a circuit control by TTL logical elements. Circuit operation with PSPICE software has been simulated. A microprocessor system with PIC18F252 microcontroller has been developed which can perform the function of the three circuits.

II. DEFASED PULSE GENERATOR

Fig. 1 shows a circuit for obtaining dephased pulses. D trigger is used to switch on the rising edge.

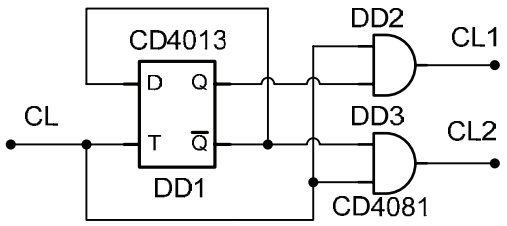

Fig. 1

Fig. 2 shows the time charts of the simulated operation of the circuit. A clock signal, two trigger output and the output signal CL2 in larger scale are shown. From the time chart it is seen that, due to delays in switching the logical elements incorrect output effects are obtained that may impair the operation of digital devices using such a generator.

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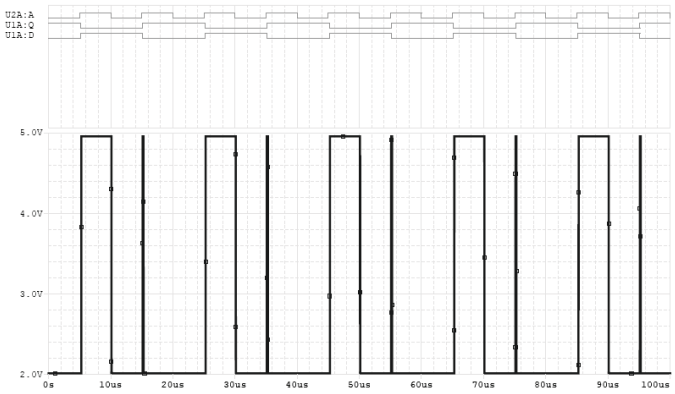

Fig. 2

III. RECTANGULAR PULSE GENERATOR WITH VOLTAGE CONTROL

Fig. 3 shows the circuit of the generator.

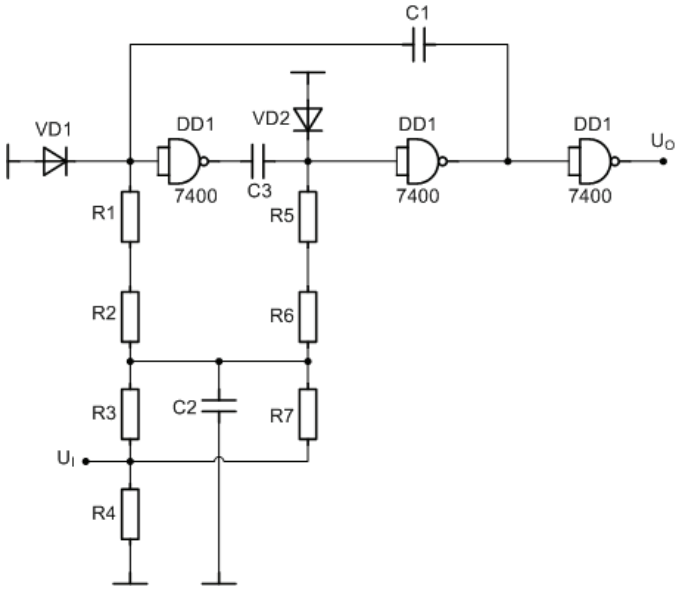

Fig. 3

Frequency variation range depends on the values of the elements C1, C3, R1, R2, R3, R5, R6, R7 the control input voltage is applied from 0 to 1 V. Fig. 4 and 5 show the time chart of the system at two different voltages 0 V - Fig. 4 and 0.8 V - Fig. 5.

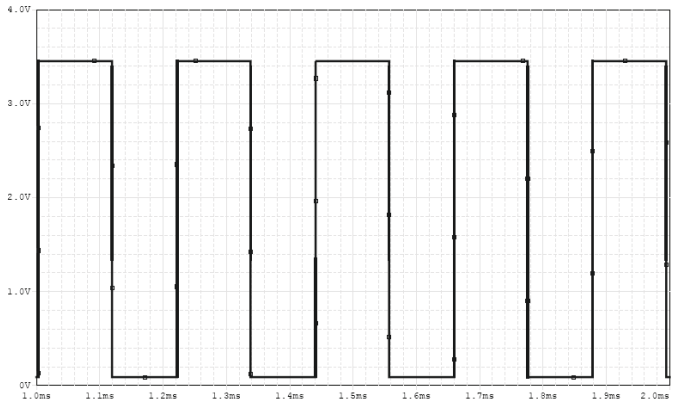

Fig. 4

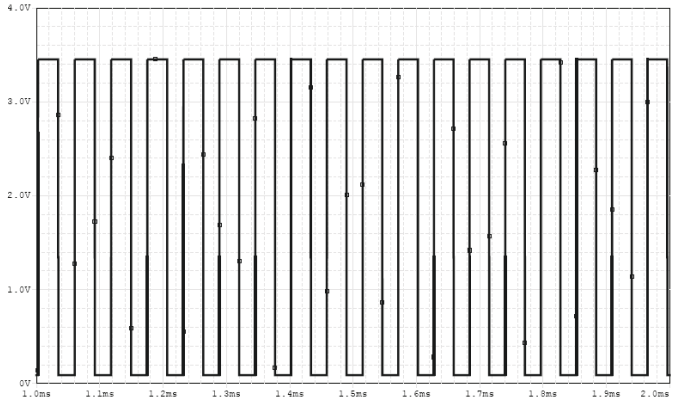

Fig. 5

The frequency can vary within wide limits. Table I gives the generator frequency at different input voltages.

TABLE I

voltage	time	frequency
0 V	218 µs	4.578 kHz
0.1 V	207 µs	4.831 kHz
0.2 V	193 µs	5.181 kHz
0.3 V	180 µs	5.556 kHz
0.4 V	158 µs	6.329 kHz
0.5 V	132 µs	7.576 kHz
0.6 V	107 µs	9.346 kHz
0.7 V	82 µs	12.20 kHz
0.8 V	56 µs	17.86 kHz
0.9 V	31 µs	32.26 kHz

Fig. 6 gives a diagram of generator frequency variation as a function of input control voltage. The disadvantage of this generator is that the dependence is nonlinear, but exponential. The input voltages frequency near 1 V is unstable. It changes at a very little change in the control voltage.

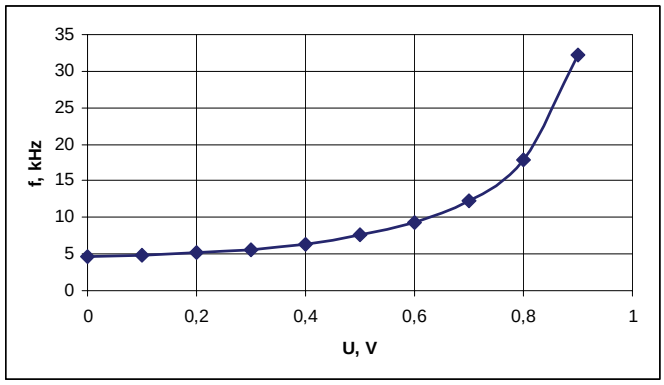

Fig. 6

IV. FREQUENCY DIVIDER

The frequency divider is developed with an adjustable division coefficient in Fig. 7.

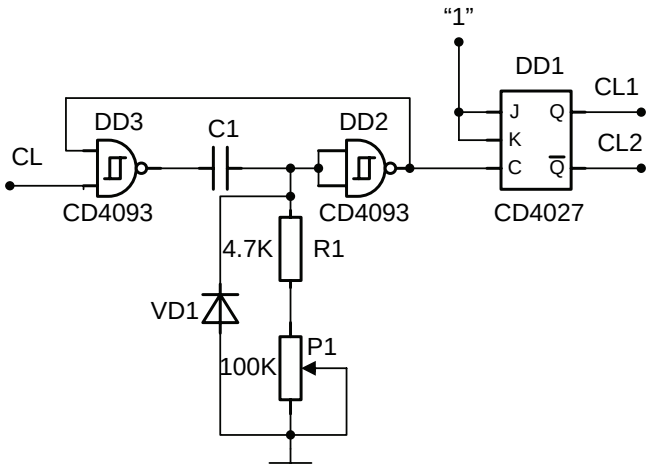

Fig. 7

Division coefficient may be modified a very wide range by adjusting the resistance of potentiometer P1. The divider is made on the bases of two logical elements AND-NOT. JK bistable is used to form the output pulses. The two elements form a monostable multivibrator. In the initial state of circuit operation condenser C1 isn't charged and the input of logic element DD2 is going to have a logical "1" as well as at the output of DD3. At that time, the output of DD2, which is connected to one input of DD3 has a logical "0" and the input clock pulses aren't get pass a pulse. The condenser is charged by the output of logic element DD3 through the resistor R1 and potentiometer P1. Once it is loaded DD2 switches and its output has high level. This enables the get pass a pulse of input pulses. When a pulse input condenser is quickly discharged in diode VD1 and the process is repeated. The time in which input pulses get pass a pulse is determined by constant of C1, R1 and P1, and this determines the coefficient of division. Fig. 8 and 9 show the time charts of operation of the circuit for division ratios of 2 and 6. The input pulses, the output pulses and the voltage condenser are given. Signal generator with PIC18F252.

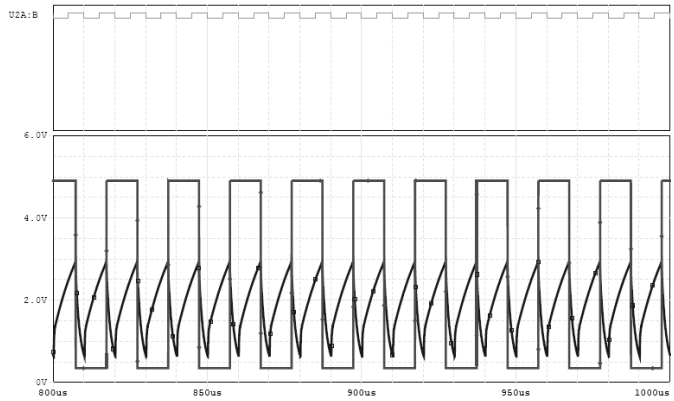

Fig. 8

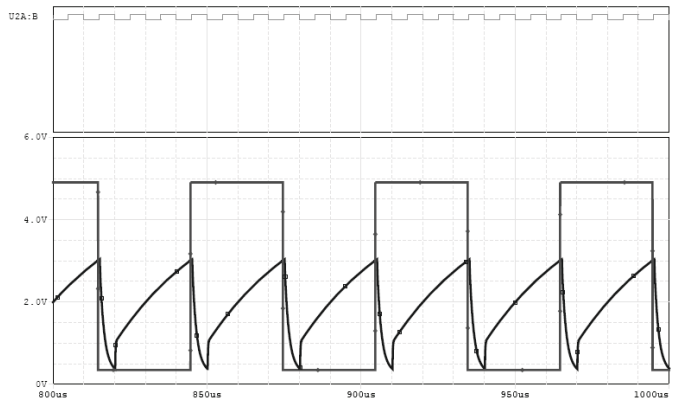

Fig. 9

V. SIGNALS GENERATOR WITH PIC18F252

Generator circuit is shown in Fig. 10

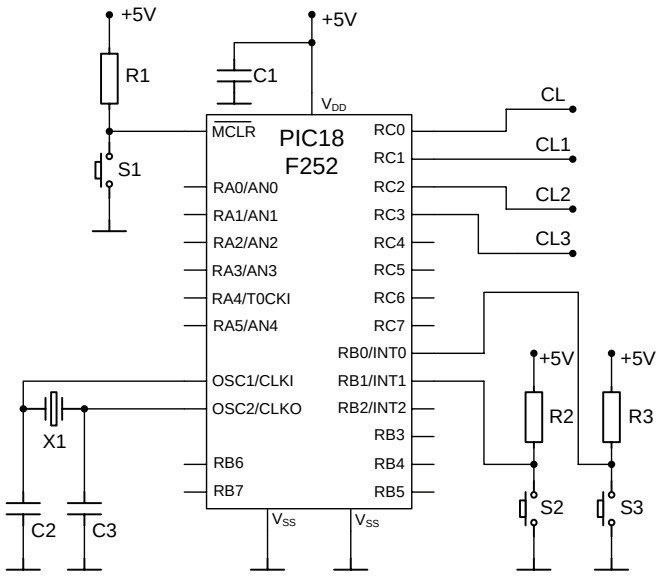

Fig.10

Generator is developed on the bases of PIC18F252 single-chip microcontroller. It can generate four output signals and has two buttons to control the operation modes. An advantage of the circuit is that the external elements necessary for the operation of the microcontroller are a very small number.

The characteristics of the chosen microcontroller are given in Table II.

TABLE II

Program memory capacity	32 K
Available I / O ports	PORT A, B, C
RAM memory capacity	1536
Number of sources of interruption	17
Number of channels of analog-digital converter	5
Body/Casing/	28 pin DIP
EEPROM memory capacity	256
Timers	4
Maximum clock frequency	40 MHz
CCP modules	2
Modules in series communication	MSSP, USART
Number of instructions	75

A program has been developed in assembly language by which the microprocessor system can cover the functional capacity of the generators discussed above. Control button S2 can switch different generators, and control button S3 sets the parameters of the generated signals.

Some of the shortcomings of the circuits discussed above have been avoided in this generator.

The time charts of the operation generator signals PIC18F252 are given in Fig.11, 12 and 13.

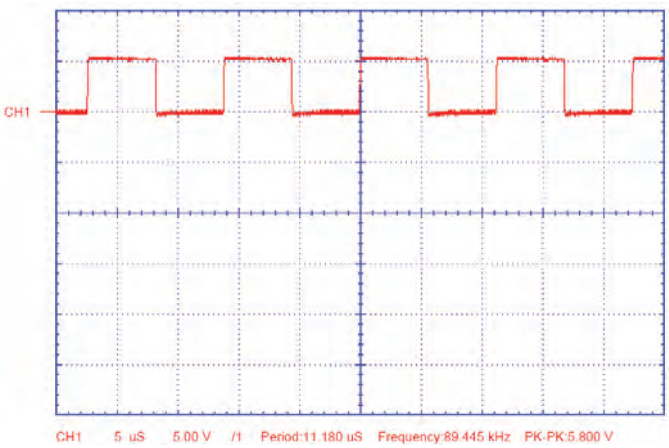

Fig. 11

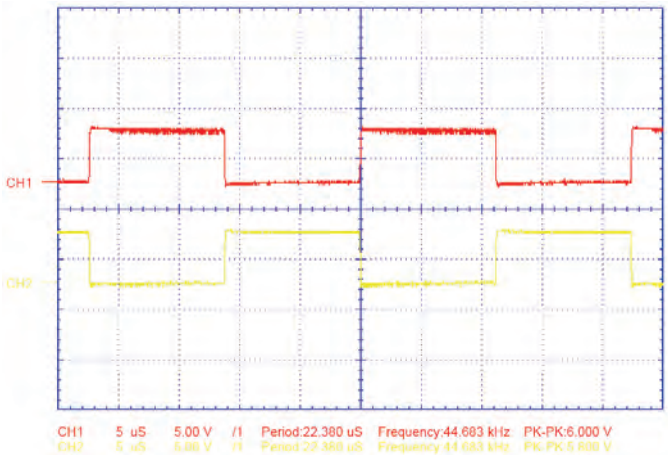

Fig. 12

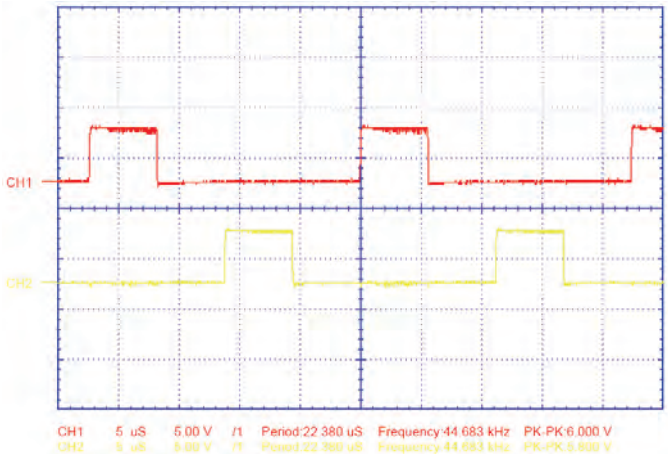

Fig. 13

VI. CONCLUSION

The proposed circuits have been developed and tested using PSPICE software. The developed of digital synchronizing signals with PIC18F252 microcontroller can find application in synchronous digital devices that require clock control signals in telecommunication.

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