High Efficiency RF Amplifier Design for Maximum PAE

Iliya Nedelchev[1]

Abstract **– In most cases during analyzing and designing efficient RF amplifiers ideal switch model is used. This model does not take in the account the power dissipation in the driving loop and its increasing with the frequency. Finally the amplifier gain cannot be determined correctly and it is obvious contradiction between a significant gain and high drain efficiency. To express the input, output and DC power simplified model of MOSFET was used allowing to design high efficiency class E amplifier with maximum PAE(power-added-efficiency). Presented are results of designing of high efficiency RF amplifiers with output power Po=100W and operating frequency 1 and 3 MHz.**

Keywords **– Power amplifier class E, High efficiency, Power-added-efficiency (PAE).**

I. Introduction

Class E resonant power amplifier becomes more attractive in recent development in wireless communications as high efficient transmitter. Lack of new theoretical investigations can be partially explained with the fact that there is no easy implemented standardize techniques for analyzing the schematic. There are many authors who are treating the active device as an ideal switch [3, 7, 8]. The optimal operating conditions of the high efficiency amplifier can be found in [3]. Analytical method for calculating the components of the output loop of the class E amplifier using ideal switch is presented in [8].

In a HF band the parasitic components and related decrease in conductivity are strongly effecting the operation. When using the ideal switch as a model usually the driving power of the real switch is neglected. Even more the model does not include the active conductance of the transistor reflecting the drain efficiency in HF region.

There is a contradiction between high gain and high drain efficiency. By that reason new systematically build method is presented where the effect of the parasitic component of the transistor and drain efficiency are taken in the account. For the mathematical equations for input, output and DC power simplified model has been used. That allows optimization of class E power amplifier with maximum enhanced efficiency PAE. The followed design is limited to FETs only.

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II. Systematically Design Method

A. Simplified MOSFET model

Simplified model of MOSFET including the parasitic components is presented on fig. 1. The ideal switch is replaces with active conductance component. The source resistance R_S was neglected in the course of the analysis from GS and DS

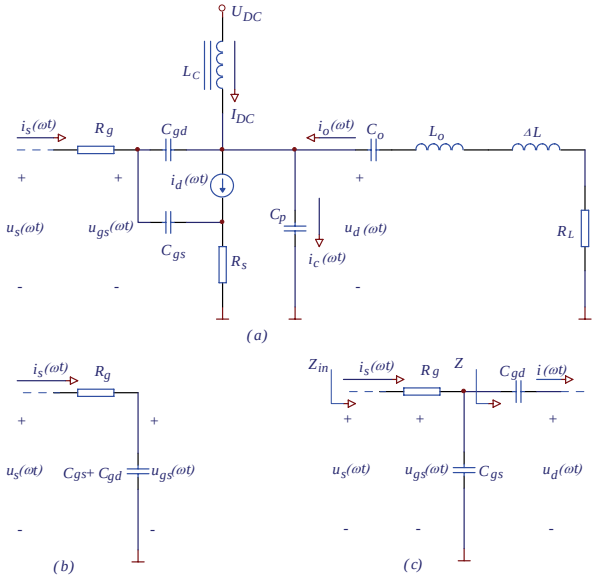

Fig.1 MOSFET model of amplifier class E (a). Equivalent circuits for positive (b), and negative (c) half-cycles.

capacitances as very low value component. Results comparisons for the input power, output power PAE etc.

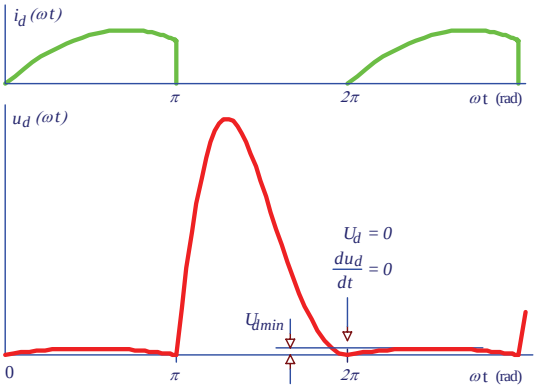

Fig. 2.Drain current and voltage waveforms for class E amplifier

confirm that connecting the capacitances to the ground does not affects the model accuracy.

Drain current and voltage as per optimal mode class E with real MOSFET are shown on fig. 2.

Mathematical expressions for drain current and voltage for class E amplifier for both state of the transistor (OFF and ON) are given in [7]. In the expressions there are additional sub-expressions added to represent the effect of the voltage drop of the sores resistor and minimum drain voltage in the ON state of the transistor ($U_{d\,min}$ –fig. 2).

The max voltage on the drain can be calculated from [5].

$$U_{d\max} = 1.13\frac{I_{DC}}{\omega C_d} + U_{d\min} + 2I_{DC}R_s\,. \qquad (1)$$

In the investigation the transistor is represented as a current source driven by voltage, where the driving voltages are gate-source and drain-source (fig. 3). This allows the DC current through the loop I_{DC} and the drain-source voltage in the ON time ($U_{d\,min}$) to be calculated [1]:

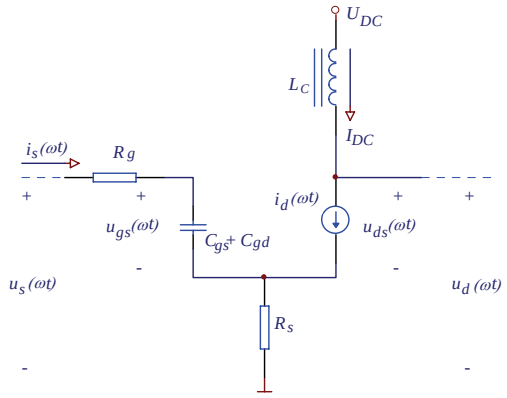

Fig. 3. MOSFET equivalent circuit.

$$I_{DC} = \frac{\pi\omega C_p\left(U_{DC} - U_{d\min}\right)}{1 + 2\pi\omega R_s C_p}, \qquad (2)$$

$$U_{d\min} = -\frac{b + \sqrt{b^2 - 4ac}}{2a}$$
$$a = 1 - 2\pi\omega R_s C_p$$
$$b = 2\left\{2\pi\omega R_s C_p\left[U_{DC} - u(\pi)\right] - 2\pi\omega C_p\frac{L}{KW} - u_{gs}(\pi)\right\} \qquad (3)$$
$$c = 4\pi\omega C_p\frac{L}{KW}U_{DC}$$

where W, L and K are the width, length and internal conductivity coefficient of the MOSFET channel.

B. Maximum PAE Design

The algorithm consists of series of steps for designing of high efficiency RF amplifier with maximum PAE and is presented on fig. 4. The data used for the design are output HF power in the load P_o, power supply DC voltage U_{DC} and operating frequency f_o.

For calculating of the components values based on design data (P_o, U_{DC}, f_o) is required R_{on} but as well C_p and $\omega_o C_p R_{on}$ to be establish. Also the parasitic parameters of the MOSFET are used.

From the design data initial calculations are used for the load resistance R_{init} and the capacitance of C_p, max current of the drain $I_{d\ max}$, and max drain voltage $U_{d\ max}$. For high efficiency operation the max MOSFET resistance in ON time is determine $R_{on\ max}$. Depending of the results MOSFET is chosen [4].

To check the right MOSFET choice the simplified model can be used. For that purpose the power gain is calculated from [1]:

$$G_p = \frac{6.935 I_{DC}^2 R_L\left[1 + \left(\frac{\omega_o R_s C_p}{2}\right)^2\right]\left[1 + \left(\omega_o R_g C_g\right)^2\right]}{U_s\omega_0^2 R_g C_g\left(2U_s C_g + U_{d\max} C_{gd}\right)}, \qquad (4)$$

where $C_g = C_{gs} + C_{gd}$.

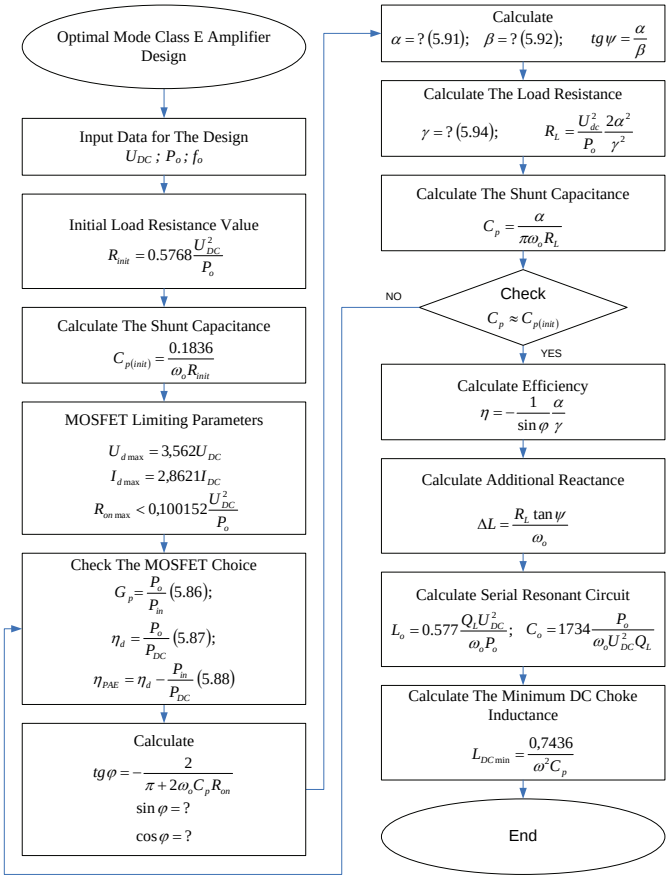

Fig. 4.Design Algorithm

The electron efficiency η_d and PAE are calculated [5].

$$\eta_d = \frac{P_o}{P_{DC}} = 1.734 \frac{I_{DC} R_L \left[1 + \left(\frac{\omega_o R_s C_p}{2}\right)^2\right]}{U_{DC}}, \quad (5)$$

$$\eta_{PAE} = \frac{P_o - P_{in}}{P_{DC}} = \eta_d - \frac{P_{in}}{P_{DC}} \quad (6)$$

$$= 1.734 \frac{I_{DC} R_L \left[1 + \left(\frac{\omega_o R_s C_p}{2}\right)^2\right]}{U_{DC}} - \frac{U_s \omega^2 R_g C_g \left(2U_s C_g + U_{d\max} C_{gd}\right)}{4 I_{DC} U_{DC} [1 + (\omega_o R_g C_g)^2]}.$$

MOSFET has been chosen in order to achieve max PAE (η_{PAE}). Limiting Conditions in this case are the max drain current $I_{d\ max}$, max drain voltage $U_{d\ max}$, and max resistance of the MOSFET in the ON state $R_{on\ max}$. After the choice of the MOSFET the coefficients are calculated [2].

$$\alpha = 2\sin^2\varphi - 2\cos^2\varphi - \pi\sin\varphi\cos\varphi - 2\omega_o C_p R_{on}\sin\varphi\cos\varphi - \frac{\pi}{2}\omega_o C_p R_{on} \quad (7)$$

$$\beta = \pi\sin^2\varphi + 4\sin\varphi\cos\varphi + \frac{\pi}{2} + 2\omega_o C_p R_{on}\sin^2\varphi \quad (8)$$

$$\gamma = 2\omega_o C_p R_{on}\cos\varphi - 3\omega_o C_p R_{on}\pi\sin\varphi - \frac{\pi^2}{2}\sin\varphi - 2\sin\varphi - \pi\cos\varphi. \quad (9)$$

The load resistance R_L and the capacitance of C_p are calculated again in comparison with the initial calculations. If the values are similar next steps of the design process can be carried out (fig. 4). If not the case, new transistor has to be selected and the design process repeats.

III. Simulation and Experimental Results

The propose design method is applied when design class E power amplifier with design data: P_o = 100 W, U_{DC}= 96 V, f_o= 1 MHz и f_o = 3,5 MHz. The component values calculated are compared with other classical methods [3], [7] results, barely different from each other and are presented in table I and II. Selected was MOSFET transistor IRF 730, V_{DSS} = 400 V, $R_{DS(on)}$=1,0 Ω, I_D = 5,5 A, C_{iss} – Input Capacitance – 700 pF, C_{oss} – Output Capacitance – 170 pF, C_{rss} – Reverse Transfer Capacitance – 64 pF.

TABLE I
AMPLIFIER CLASS E – 3.5 MHZ

Parameter	Suggested method	Classic method	Difference [%]
$\Delta L\ [\mu H]$	6,796	9.167	34,89
$C_p\ [pF]$	577	584	1,12
$L_o\ [\mu H]$	42,32	30,62	-27,65
$C_o\ [pF]$	599	827	38,06
$L_{DC}\ [\mu H]$	180	180	0
η_d [%]	97,4	90,2	-7,39
η_{PAE} [%]	96,1	88,9	-7,49
$G_p\ [dB]$	46,9	32,6	-30,49

TABLE II
AMPLIFIER CLASS E – 1 MHZ

Parameter	Suggested method	Classic method	Difference [%]
$\Delta L\ [\mu H]$	1,934	2,62	35,47
$C_p\ [pF]$	164	180	9,76
$L_o\ [\mu H]$	12,09	8,749	-24,51
$C_o\ [pF]$	178	236	32,58
$L_{DC}\ [\mu H]$	50	50	0
η_d [%]	96,3	87,1	-9,55
η_{PAE} [%]	94,7	85,7	-9,50
$G_p\ [dB]$	44,7	30,5	-30,77

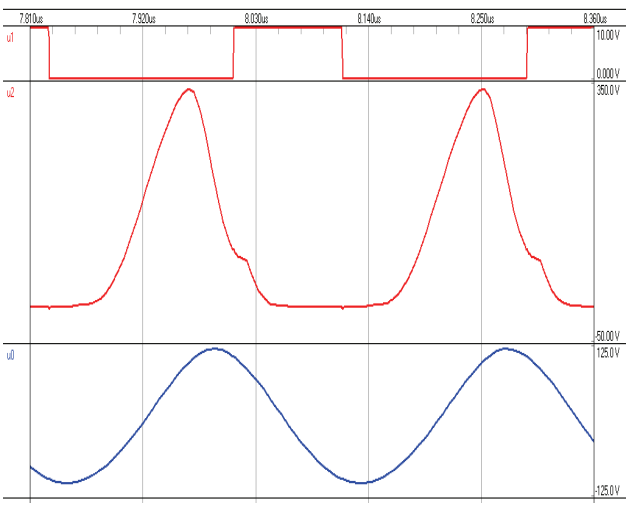

Fig. 5. Amplifier class E voltage waveforms.

The results were checked with computer simulation with Protel 99 SE at operating frequency 3.5MHz. The gate voltage *u1*, drain voltage *u2* and load voltage *u0* presented are on fig. 4. The shape of the waveforms confirms that all optimal conditions for class E operation are met.

Output voltage by default is sine wave but contains about 6% second harmonic. It distort the waveform THD 6.7% (fig. 6). If special output voltage waveform requirements higher order filter can be connected after the series resonant loop in order to suppress the high level harmonics and match the output impedance of the amplifier to the load. As sample application, it can be used as a quadrature modulator in coaxial cable distributed television networks. [6].

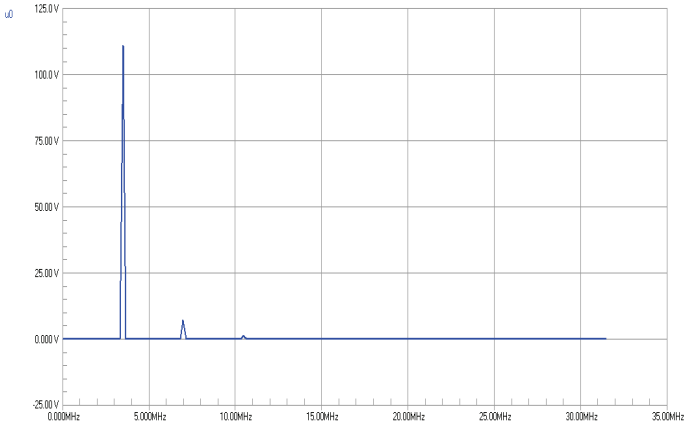

Fig. 6. Load voltage spectrum.

Based on the design prototype unit was developed. Pictured are the drain and load waveform of power amplifier class E operating at 1MHz (fig. 7).

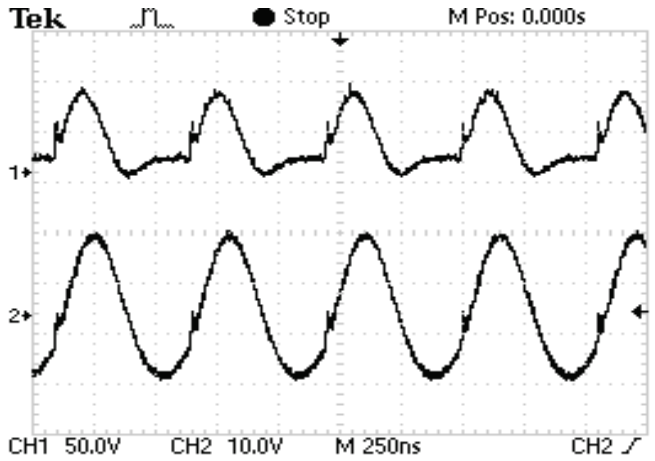

Fig. 7. Waveform of class E:
1 - Drain voltage, 2 - Load voltage.

As can be seen the amplifier class E is in stable operation and all theoretical conditions for optimal mode and minimal losses are met.

IV. Conclusion

The method presented reflects the transistor parameters. That allows by the choice of the MOSFET to compromise between bigger efficiency of the drain (η_D) i.e. minimum ON resistance R_{on} or bigger power gain G_p i.e. small transistor input capacitor C_{iss}. That decreases the driving power, allowing to improve the current and temperature stress of the driving stage and increase the power – added efficiency (η_{PAE}).

When calculating the shunt capacitor value C_p the transistor parameters are taking into a account as well, allowing minimizing the losses and improve the efficiency and maximum operating frequency where the described transistor can be used.

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