A 6–9 GHz Resistive Feedback Low Noise Amplifier Designed in 0.18µm CMOS Technology

Alena Djugova[1], Jelena Radic[2] and Mirjana Videnovic-Misic[3]

***Abstract* – In this paper two-stage low-noise amplifier (LNA) designed for operation over the common frequency range, 6–9 GHz, allocated for ultra-wideband (UWB) communications both in USA, Europe, and Japan is presented. Implemented in 0.18µm CMOS technology, it features a maximum gain (S_{21}) of 17.89 dB dissipating only 6.5 mA from the 1.8 V supply. In addition, LNA shows less than –10 dB input return loss (S_{11}) and less than –14.33 dB output return loss (S_{22}). The noise figure (NF) ranges from 3.29 dB to 3.68 dB over the band of interest. The high circuit stability parameters K_f > 37.24 and B_{1f} > 0.98 are obtained.**

***Keywords* – Ultra-wideband (UWB), Low noise amplifier (LNA), Resistive shunt-feedback topology.**

I. INTRODUCTION

Ultra-wideband (UWB) presents low power technology applicable for short-range, high-speed wireless communications. UWB differs from other communication techniques due to employing extremely short-time pulses (sub-nanosecond) to communicate between transmitters and receivers. The short duration of UWB pulses generates very wide bandwidth (GHz) in frequency domain. According to the rules set defined by the US Federal Communications Commission's (FCC) in 2002, allocated band for the unlicensed use of UWB devices is between 3.1 GHz and 10.6 GHz frequency range [1]. In order to protect the existing radio services from UWB interference maximum allowed power spectral density is –41.3dBm/MHz. Compared to the FCC in United States, the regulatory bodies in Europe decided on more stringent emission masks and specific restrictions. As frequency band from 3–5 GHz is allocated to the fixed services/WiMax systems, unrestricted frequency range in Europe is between 6 GHz and 8.5 GHz. Meanwhile in Japan and Korea, only band from 7–9 GHz is released without restriction. In addition, standard for the UWB spectrum in China, with frequency band from 6–9 GHz, will be allocated soon. Thus, frequency range of 6–9 GHz is the most interesting for UWB systems with worldwide usage.

One of the demanding tasks in up-to-date receiver design is design of low noise amplifier (LNA). As first circuit in the receiver's chain it needs to fulfill several stringent requirements. Sufficient gain is obligatory to amplify received weak signal and to overcome the noise of the subsequent stages, adequate input and output matching, to minimize reflection, and low noise figure (NF), to improve sensitivity. All this have to be obtained within defined bandwidth and with low power consumption.

In Section II basic circuit design techniques for obtaining wide frequency operational bandwidth, are described, while chosen broadband LNA architecture, two-stage common-source resistive shunt-feedback based topology, is analyzed in Section III. Simulated figures of merit (FOMs) are given in Section IV followed by discussion and comparison with other UWB LNA designs found in literature. The Section V concludes the paper.

II. BROADBAND LNA DESIGN TECHNIQUES

Four major UWB LNA's design approaches have been reported in literature: distributed amplifier, common-gate circuit, inductively degenerated common-source amplifier with additional multistage input filters and common-source amplifier with resistive shunt-feedback technique.

A. Distributed Amplifier (DA)

The renewed interest in distributed circuits arises mainly due to the capability of designing on-chip transmission lines (realized using either coplanar waveguides or cascaded LC circuits) and high-Q inductors. The general block diagram of a DA comprises transmission lines and gain stages distributed along them. Whit this architecture impedance matching over a wide bandwidth as well as a broadband gain, equal to the sum of the scalar gains from each stage, can be achieved. Consequently, this approach is power hungry and area consuming. Moreover, NF optimization for this technique is still an issue [2].

B. Common-gate Amplifier

The input common-gate stage provides the wideband input impedance matching with less design complexity and small area occupancy. However, the main disadvantage of this type of amplifier is high noise figure (noise from the load network and channel thermal noise are referred to the input in their entirety limiting the minimum possible noise figure). As input matching is coupled with noise matching, noise canceling methods need to be used. Additionally, their relatively low transconductance value can not provide low noise and high gain in a whole frequency range. This type of amplifier is

[1]Alena Djugova is with the Faculty of Technical Sciences, Trg Dositeja Obradovica 6, 21000 Novi Sad, Serbia, E-mail: alenad@uns.ac.rs.

[2]Jelena Radic is with the Faculty of Technical Sciences, Trg Dositeja Obradovica 6, 21000 Novi Sad, Serbia, E-mail: jelenar_@uns.ac.rs.

[3]Mirjana Videnovic-Misic is with the Faculty of Technical Sciences, Trg Dositeja Obradovica 6, 21000 Novi Sad, Serbia, E-mail: mirjam@uns.ac.rs.

usually combined with additional amplifying stage which provides high-frequency gain and enhances the amplification bandwidth [3].

C. Inductive Degenerated Common-Source Amplifier Incorporated with Passive Input Matching Networks

Input multistage reactive network of the amplifying device is embedded in a multi section filter structure so that the overall input reactance is resonated over the whole band from 3.1 to 10.6 GHz. Inductive source degeneration is used for proper input matching and the size of the transistor is no longer coupled to the impedance matching requirement. Therefore, gain flatness and low power consumption are achieved. The main drawbacks of this approach are the large silicon area occupied by the integrated inductors of the passive networks and the noise contribution introduced by the passive elements at the input of the LNA. The NF rises rapidly at high frequencies, consequently decreasing the receiver sensitivity in the higher UWB bands [4]. In addition, the high-quality-factor integrated inductors require high accuracy of the electromagnetic design, and the traditional mismatch reduces the design reliability.

III. Resistive Feedback Based LNA Circuit Design

The proposed wideband LNA is shown in Fig. 1. Proper input matching over the whole band is achieved with resistive shunt-feedback technique in both stages. This technique provides wideband input matching and flat gain [5]. Additionally the inductive series-peaking technique is adopted in the input terminal of the output stage. The source follower output buffer is used as a low output impedance (i.e., 50Ω) interface.

All bias circuits are composed of resistors R_{biasn} and R_{refn}, n = 1, 2, 3, and transistor M_n, n = 5, 6, 7, where transistor forms DC current mirror with corresponding transistor (M_1, M_2, M_4). To decrease the overall power consumption (P_D), bias transistor width, should be small fraction of amplifying transistor width. The R_{biasn} value is chosen large enough to provide high impedance path to the RF signal while making a small contribution to the circuit noise.

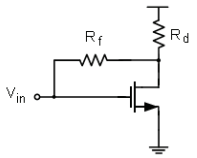


Fig. 2. Common source LNA with resistive feedback

Capacitors C_g and C_b are input and output DC blocking capacitors. Their values are chosen large so they do not influence the resonant frequency of the input and output circuit, respectively.

A. Input Stage

The first block of the proposed LNA topology can be roughly seen as basic common source amplifier with resistive shunt-feedback, shown in Fig.2. R_{f1} forms resistive shunt-feedback and drain impedance is equal to: $Z_D = j\omega L_{d1}$, hence input resistance is given by:

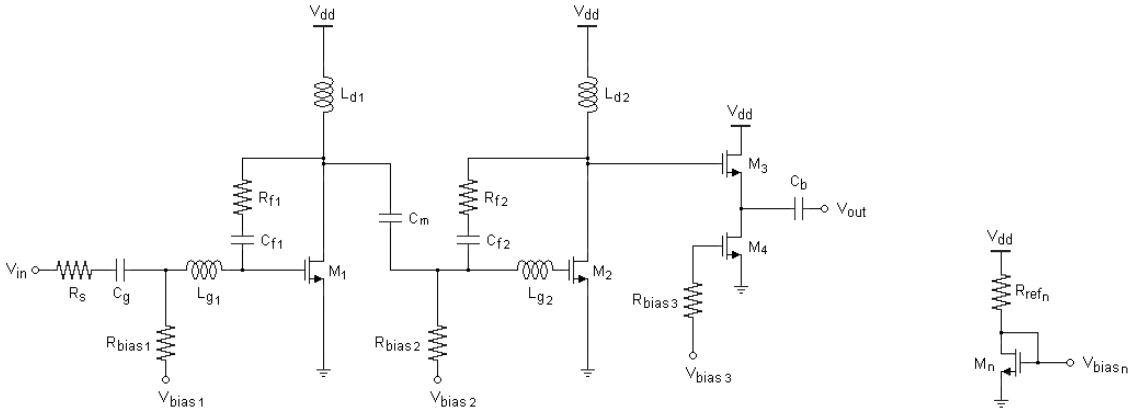
$$R_{in} = \frac{R_{f1} + Z_D}{1 + g_m \cdot Z_D}. \tag{1}$$

Increase in value of feedback resistor, R_{f1}, results in R_{in} increase. Therefore, to obtain 50Ω input match, feedback resistor tends to be a few hundred ohms, which leads to significant NF degradation.

Therefore, additional degree of freedom is provided by the gate inductance L_{g1}. Miller equivalent input resistance of R_{f1} is approximately given by [6]:

$$R_{feq} = \frac{R_{f1}}{(1 - A_v)} \tag{2}$$

where A_v is the open-loop voltage gain of the first LNA stage. With this transformation Q-factor of the input circuit shown in Fig. 1 is given by:



(a) (b)

Fig. 1. The designed 6−9 GHz CMOS LNA: (a) amplifying circuit, and (b) biasing circuit

$$Q = \frac{\omega_0 \cdot L_{g1}}{R_{feqs}} \tag{3}$$

where $R_{feqs} = \dfrac{R_{feq}}{(Q_p^{\ 2} + 1)}$ and $Q_p = R_{feq} \cdot \omega_0 \cdot C_{gs}$.

Decreasing value of inductor L_{g1} Q-factor is lower and higher bandwidth occurs.

Simultaneously impedance and noise matching over the band of interest is achieved by appropriately selected values of L_{g1}, R_{f1}, and the size and bias of the input transistor M_1, i.e. C_{gs1} and g_{m1}.

Voltage gain of resistive feedback based LNA is equal to:

$$A_v \approx -\frac{g_m \cdot R_{f1} \cdot Z_D}{R_{f1} + g_m \cdot R_s \cdot Z_D} = -\frac{1}{\dfrac{1}{g_m \cdot Z_D} + \dfrac{R_s}{R_{f1}}}. \tag{4}$$

Due to strong dependence of voltage gain on the amplifying transistor transconductance, the amplifier with resistive feedback requires a large amount of current to achieve high gain. Also, it can be seen from (4), that parameter R_{f1} increase results in voltage increase.

Combined with parasitic capacitances, purely resistive loads would result in limited high frequency performance. Thus, inductive load, L_{d1}, is used to increase bandwidth and improve gain flatness. In addition value of L_{d1} determines the gain of the first stage.

Coupling capacitor C_m is used to couple RF signal from transistor M_1 to transistor M_2.

B. Second Stage

The second stage is another common-source resistive feedback based stage. A peaking inductor L_{g2} is added to the gate-terminal of M_3 for LNA gain and NF improvement at high frequencies. Inductor L_{d2} resonate with the total parasitic capacitance at the drain of M_2, and determines the gain of the second stage and flat gain.

IV. Simulation Results

The designed circuit has been simulated in UMC 0.18µm CMOS six-metal technology using Spectre Simulator from Cadence Design System. BSIM3V3 models for all circuit components were introduced.

LNA topology was optimized with the main aim to obtain proper input matching, high flat gain, while minimizing P_D, *NF* and keeping acceptable values for remaining FOMs. Simulation results for two-stage resistive feedback LNA topology are given in Figs. 3–5 (S_{11} and S_{22}, S_{21}, *NF* and NF_{min}).

Parameter S_{11} is below –10 dB in the band of interest (–13.36 dB at 6 GHz and –10.41 dB at 9 GHz). This demonstrates the effectiveness of wideband input matching obtained by resistive feedback topology. Decrease in R_{f1} value

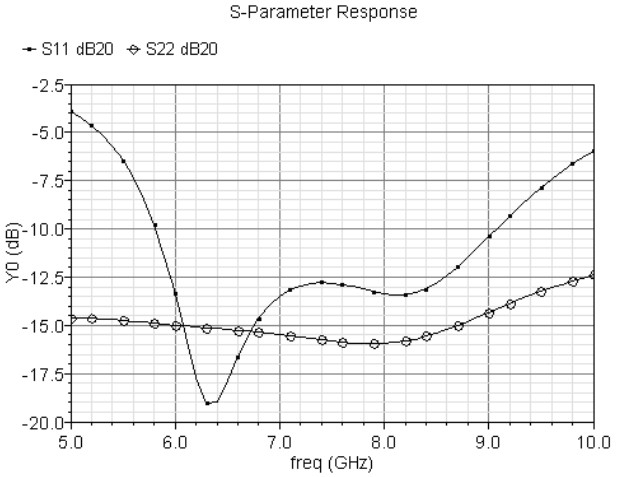


Fig. 3. LNA input (S_{11}) and output (S_{22}) return loss

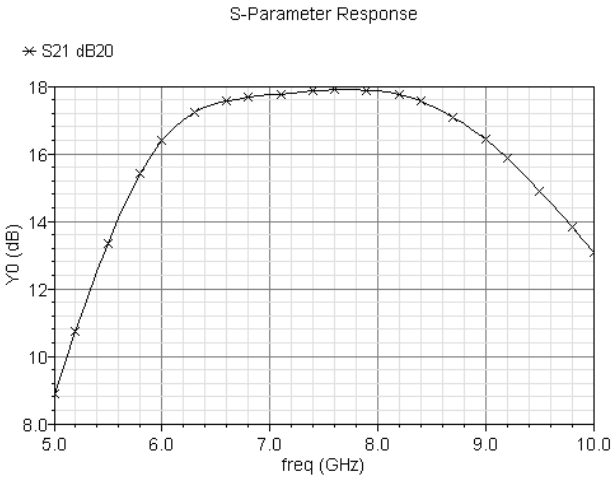


Fig. 4. LNA gain (S_{21})

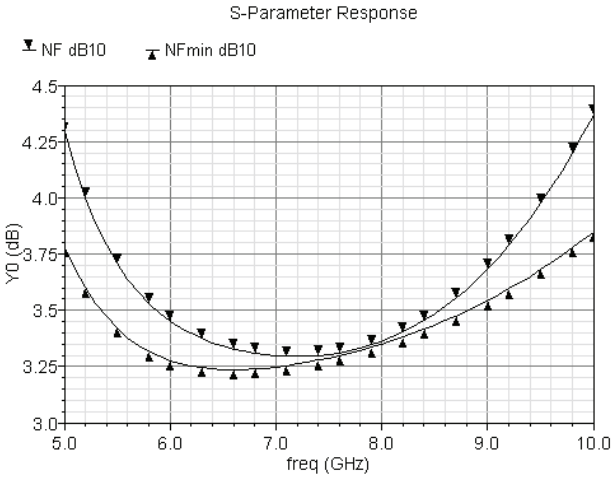


Fig. 5. LNA noise figure (*NF*) and minimum noise figure (NF_{min})

results in lower S_{11} value and higher bandwidth, while decrease in L_{d1} inductor value shifts S_{11} to higher frequencies and reduces minimum S_{11} value. L_{g1} increase narrow the S_{11} characteristic, therefore trade-off between its value and wanted bandwidth has to be achieved. Parameter S_{22} is less than –14.33 dB for the whole simulated range. This is achieved by enhancement LNA topology with output buffer.

Further excellent reverse isolation (S_{12}) below –55.45 dB is obtained. Regarding the gain, maximum S_{21} parameter value of 17.89 dB is achieved at 7.7 GHz (16.38 dB at 6 GHz and 16.42 dB at 9 GHz). Variation in S_{21} value in band of interests is 1.51 dB and the 3-dB bandwidth covers frequency range from 5.72 GHz to 9.5 GHz. Widths of amplifying transistors M_1 and M_2 determines the LNA gain while higher values of resistors R_{f1} and R_{f2} improve it. Transistor values are chosen to satisfy the gain requirement, while keeping at the same time P_D at reasonable level.

NF exhibits small variation (up to 0.39 dB) across entire simulated band (3.45 dB at 6 GHz and 3.68 dB at 9 GHz). Minimum NF value of 3.29 dB is obtained at 7.2 GHz. NF values are close to NF_{min}, the minimum possible NF values (3.28 dB at 6 GHz and 3.54 dB at 9 GHz).

For voltage supply of 1.8 V, LNA core consumes 6.5 mA. The rest is consumed by the output buffer (2.84 mA) and biasing circuits (3.98 mA).

Unconditional stability requirements for the whole simulated range are satisfied. Minimum values for stability factors K_f (Rollet stability factor) and B_{1f} (alternate stability factor) are equal to 37.24 and 0.98, respectively, which are values much higher than 1 and 0 [7], [8].

The optimized FOMs of the designed LNA and FOMs values of similar LNA topologies found in literature are summarized in Table I. In comparison with the amplifier design presented in [9], proposed LNA circuit in this paper dissipates something higher amount of power, gives larger gain and better input matching. Furthermore, LNA in [9] achieves the wideband input matching by a three-section band-pass Chebyshev filter configuration, requiring usage of large number of reactive elements that causes higher NF and larger chip area. A CMOS dual-wideband low-noise amplifier (LNA) in [10] shows lower S_{21} and higher S_{11}. Result for higher *NF* and power consumption is due to more complex topology which consists of a wideband input impedance matching network, two stage cascode amplifiers with shunt-peaked load, a notch filter and an output buffer.

TABLE I
LNA PERFORMANCE COMPARISON

	This work	[9]	[10]	[11]
BW [GHz]	6–9	6–10	6–10.3	4.5–11
S_{11} [dB]	<–10.41	<–9	<–8.31	<–8.2
S_{22} [dB]	<–14.33	<–12	N/A	N/A
S_{21} [dB]	17.89	11.6	10.34	14.2
NF [dB]	3.68	5.3	3.8*	5.1
Power [mW]	11.7	11.6	24.07	20.4
Technology	0.18µm	0.18µm	0.18µm	90nm

* Minimum noise figure.

The same drawbacks occur in [11] where differential topology with integrated balun is used. Despite usage of technology with lower DC supply voltage (1.2 V) differential design makes this approach power hungry.

V. CONCLUSION

A 6–9 GHz two stage LNA designed in 0.18µm UMC CMOS technology for frequency band from 6 GHz to 9 GHz is demonstrated in this paper. Resistive feedback technique for ultra-wideband design is used. This technique gives adequate input match without introducing large number of additionally components (inductors and capacitors) and improves LNA gain. Obtained simulation results show high gain of 17.89 dB with consumption of only 11.7 mW while maintaining low noise figure.

ACKNOWLEDGEMENT

This research was supported by the Serbian Ministry of Science and Technological Development (contract number TR-32016).

REFERENCES

[1] G. R. Aiello and G. D. Rogerson, "Ultra-Wideband Wireless Systems", *IEEE Microwave Magazine*, vol. 4, pp. 36–47, 2003.

[2] P. Heydari and D. Lin, "A Performance Optimized CMOS Distributed LNA for UWB Receivers", *CICC'05, Conference Proceedings*, pp. 337–340, San Jose, California, USA, 2005.

[3] K. Chen, J. Lu, B. Chen and S. Liu, "An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-µm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 3, pp. 217-221, 2007.

[4] A. Bevilacqua and A. M. Niknejad, "An Ultrawideband CMOS Low Noise Amplifier for 3.1–10.6-GHz Wireless Receivers", *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2259-2268, 2004.

[5] C. W. Kim, M. S. Kang, P. T. Anh, H. T. Kim and S. G. Lee, "An Ultra-Wideband CMOS Low Noise Amplifier for 3–5-GHz UWB System," I*EEE Journal of Solid-State Circuits*, vol. 40, pp. 544-547, 2005.

[6] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York, McGraw-Hill, 2001.

[7] SpectreRF simulator, Cadence Design System, Available: http://www.cadence.com

[8] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, Prentice Hall, 1984.

[9] Y.-Ch. Chen and Ch.-N. Kuo, "A 6~10-GHz Ultra-Wideband Tunable LNA", ISCAS 2005, Conference Proceedings, vol. 5, pp. 5099–5102, Kobe, Japan, 2005.

[10] Z.-Y.Huang and Ch.-Ch.Huang, "CMOS Dual-Wideband Low-Noise Amplifier with Notch Filter for 3.1GHz–10.6GHz Ultra-Wideband Wireless Receiver", A*SICON'07, Conference Proceedings*, pp. 415–418, Guilin, China, 2007.

[11] A. Bevilacqua, C. Sandner, M. Tiebout, A. Gerosa and A. Neviani, "A 6–9-GHz Programmable Gain LNA with Integrated Balun in 90-nm CMOS", *ICUWB2008, Conference Proceedings*, vol.1, pp. 25–28, Hannover, Germany, 2008.