Influence of the Snubbers over the Work of a Transistor Resonant DC/DC Converter

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Abstract **- The work of a transistor resonant DC/DC converter is analyzed using the phase plane method, taking into consideration the influence of the snubbers, which are connected in parallel to the transistors. The author has obtained the equation of the frontier line after which are not observed the conditions for switching the transistors by zero voltage (ZVS). The frontier of the natural commutation is drawn in the plane of the output characteristics of the converter.**

Keywords **- transistor resonant DC/DC converter, snubbers**

I. INTRODUCTION

Theoretical analysis of a transistor resonant DC/DC converter, operating at frequencies, higher than its resonant frequency, is performed in a number of publications [1÷5]. Usually the influence of the protective capacitors (snubbers), connected in parallel, is neglected. The analyses describe accurately the operation of the converter but they do not allow clearing out an important fact: the increase in the load resistance leads to breakage in the conditions for natural switching the transistors on at zero voltage (ZVS) as well as to stopping the converter. The bigger the capacity of the snubbers, the earlier this failure of the commutation is observed.

The present paper clears out this phenomenon. A transistor resonant DC/DC converter is analyzed using the phase plane method, taking into consideration the influence of the snubbers.

II. ANALYSIS OF THE CONVERTER

Fig.1 presents the principal electric circuit diagram of the converter under consideration. It is assumed that all circuit elements are ideal, and the pulsations of the input and output voltages are neglected. The matching transformer Tr is also an ideal one and it has a coefficient of transformation **k**.

The following quantities in relative units are introduced:

$x = U'_C = u_C / U_d$ - voltage of the capacitor C;

$U'_0 = kU_0 / U_d$ - output voltage;

$I'_0 = \dfrac{I_0 / k}{U_d / Z_0}$ - output current;

$U'_{Cm} = U_{Cm} / U_d$ - maximum voltage of the capacitor C;

$\nu = \omega / \omega_0$ - distortion of the resonant circle

where ω is the operating frequency, and $\omega_0 = 1/\sqrt{LC}$ and $Z_0 = \sqrt{L/C}$ - are the resonant frequency and the characteristic impedance of the oscillating circuit.

All snubbers $C_1 \div C_4$ are theoretically equivalent to just one condenser with capacity C_1 (drawn by dotted line in fig. 1), connected in parallel to the input of the converter. This can be physically realized, since the semiconductor switches do not have a command for opening. They close by force but open naturally at zero voltage (ZVS).

The operation of the converter under an established mode per cycle can be divided into six consecutive stages, whose equivalent diagrams are shown in fig. 2.

The commutations of the output voltage are not instantaneous, due to the availability of the capacitor C_1. During these commutations the transistors are closed and the current in the oscillating circuit closes through the capacitor C_1 (stages 2 and 5). Then the capacitors C and C_1 are connected in series and the sinusoidal quantities have angle frequency $\omega'_0 = 1/\sqrt{LC_E}$, where $C_E = CC_1/(C + C_1)$.

It is known [3, 4] that in a phase plane only sinusoidal quantities with the same angle frequency can be presented. In order to carry out an analysis of the transistor converter, two phase planes must be used – the first one to show the operation of the converter during the intervals between the commutations of the inverter output voltage (stages 1, 3, 4 and 6), and the second one to show the operation of the converter during these commutations (stages 2 и 5).

However, the investigation of one of these commutations (stage 2) shows that it is possible to use just one phase plane to illustrate the whole period of the converter operation.

The following notations are made:

$$a = C_1 / C\,; \qquad k = \sqrt{(a+1)/a} \tag{1}$$

By the index **(B)** all quantities at the beginning of the commutation are denoted (p.$M_{(B)}$), while the same quantities at the end of the commutation are denoted by the index **E.**

The voltages of the capacitors C_S and C can be expressed by:

$$U_{Cs_{(E)}} = U_{Cs_{(B)}} + 2U_d \tag{2}$$

$$U_{C(_E)} = U_{C_{(B)}} + 2aU_d \tag{3}$$

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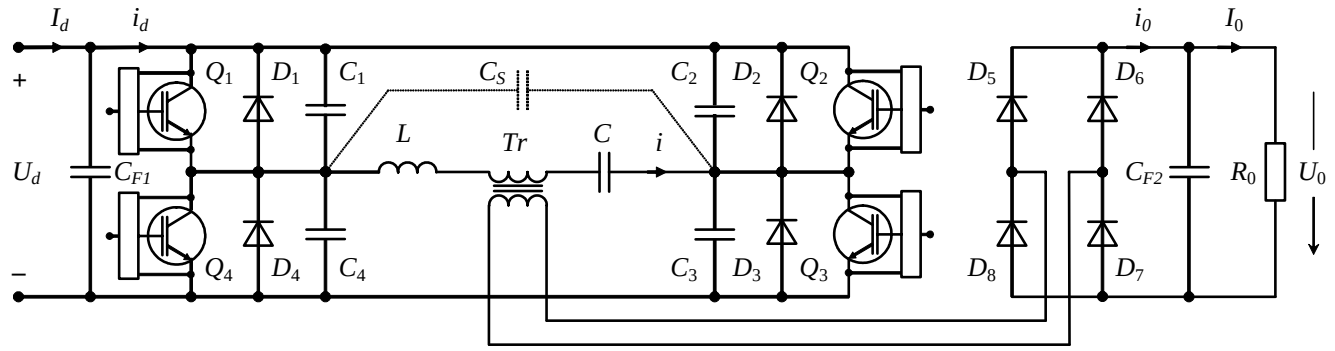

Fig.1. Circuit of the transistor DC/DC converter

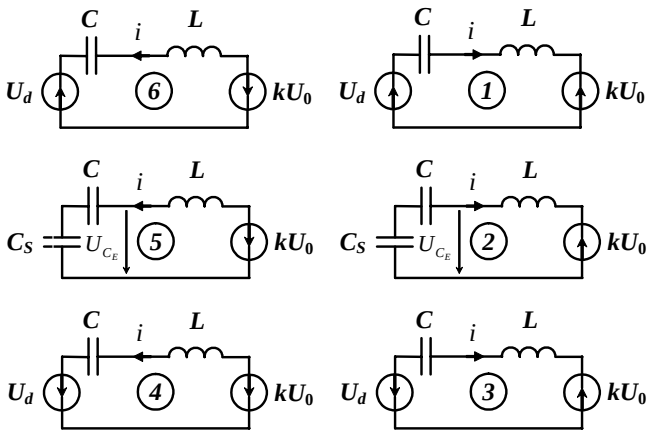

Fig.2. Equivalent circuits

The following equation is valid for stage 2:

$$\left(U_{C_E(B)}+U_0\right)^2+\left(i_{(B)}\sqrt{L/C_E}\right)^2=\left(U_{C_E(E)}+U_0\right)^2+ \\ +\left(i_{(E)}\sqrt{L/C_E}\right)^2 \tag{4}$$

From (2), (3) and (4) it is obtained:

$$\left(U_{C(B)}+U_0\right)^2+\left(i_{(B)}\sqrt{L/C}\right)^2=\left(U_{C(E)}+U_0\right)^2+ \\ +\left(i_{(E)}\sqrt{L/C}\right)^2 \tag{5}$$

or in relative units:

$$\left(U'_{C(B)}+U'_0\right)^2+I'^2_{(B)}=\left(U'_{C(E)}+U'_0\right)^2+I'^2_{(E)} \tag{6}$$

Equation (6) shows that in the phase plane $\left(x=U'_C;y=I'\right)$ the points, corresponding to the beginning (p.$M_{(B)}$) and the end (p.$M_{(E)}$) of the commutation, belong to the same arc from a circle with its center in point $\left(-U'_0;0\right)$.

It is important to note that only the ending points matter on this arc. Its central angle does not matter, as during the commutation the electric quantities change with angle frequency $\omega'_0=1/\sqrt{LC_E}$, not with $\omega_0=1/\sqrt{LC}$.

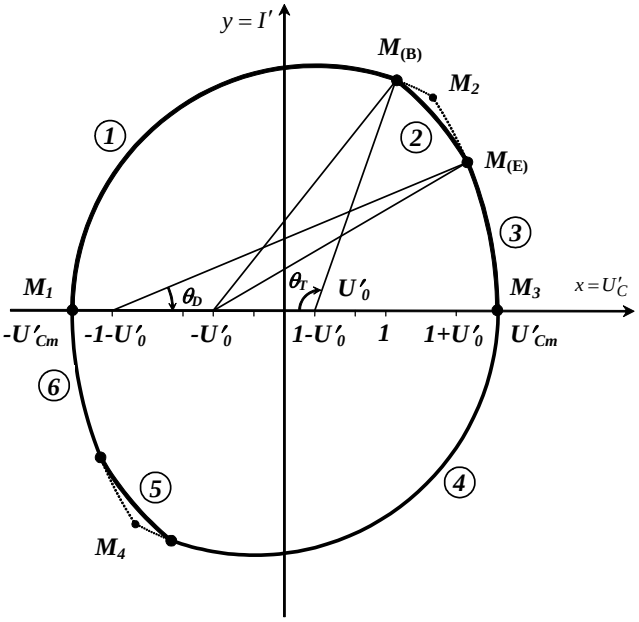

Fig.3. Trajectory of the depicting point in the phase plane

The trajectory of the depicting point in the phase plane $\left(x=U'_C;y=I'\right)$ is shown in fig.3, considering the influence of the protective capacitors on the performance of the converter. The following correlations are valid for it:

$$\left(U'_{C(B)}-1+U'_0\right)^2+I'^2_{(B)}=\left(-U'_{Cm}-1+U'_0\right)^2 \tag{7}$$

$$\left(U'_{C(E)}+1+U'_0\right)^2+I'^2_{(E)}=\left(U'_{Cm}+1+U'_0\right)^2 \tag{8}$$

Equation (3) is presented in relative units as it follows:

$$U'_{C(E)}=U'_{C(B)}+2a \tag{9}$$

From (6) and (9) it is obtained:

$$I'^2_{(E)}=I'^2_{(B)}-4a\left(U'_{C(B)}+a+U'_0\right) \tag{10}$$

The expressions (9) and (10) for $U'_{C(E)}$ are substituted in (8), then (8) is subtracted from (7) and it is obtained:

$$U'_{C(B)}=U'_0\cdot U'_{Cm}-a \tag{11}$$

$$U'_{C(E)} = U'_0 \cdot U'_{Cm} + a \qquad (12)$$

These two results are in conformity with the fact that when the protective capacitors are decreased, i.e., a→0, then p. $M_{(B)}$ and p. $M_{(E)}$ tend to p. M_2, and $U'_{C(B)}$ and $U'_{C(E)}$ tend to $U'_0 U'_{Cm}$ [3, 4].

According to fig.3 it follows:

$$U'_{Cm} = \frac{a + (1 - U'_0) \cdot (1 - \cos\theta_T)}{U'_0 + \cos\theta_T} \qquad (13)$$

$$I'_{(B)} = (U'_{Cm} + 1 - U'_0)\sin\theta_T \qquad (14)$$

$$\theta_C = \frac{1}{k}\left(arctg \frac{kI'_{(B)}}{U'_{C(B)} + U'_0 - 1} - arctg \frac{kI'_{(E)}}{U'_{C(E)} + U'_0 + 1} \right) \qquad (15)$$

$$\theta_D = arctg \frac{I'_{(E)}}{U'_{C(E)} + U'_0 + 1} \qquad (16)$$

Where θ_C is the angle of commutation, θ_T and θ_D are correspondingly the angles of conductivity of the transistors and reverse diodes in the inverter.

The average current value through the load is:

$$I'_0 = 2\nu U'_{Cm} / \pi \qquad (17)$$

where

$$\nu = \frac{\pi}{\theta_T + \theta_D + \theta_C} \qquad (18)$$

Switching the transistors Q2 and Q4 on at zero voltage is ensured if after switching Q1 and Q3 off, the protective capacitors C_2 and C_4 manage to discharge completely (the equivalent C_1 manages to recharge from $-U_d$ to $+U_d$) before the current in the oscillating circuit becomes zero. It means that p. $M_{(E)}$ (fig. 3) has to be located always above the abscissa or, in the border case, on it. From (12) the condition for natural commutation of the transistors can be written:

$$U'_{Cm} \geq U'_{C(E)} = U'_0 \cdot U'_{Cm} + a \qquad (19)$$

or $$U'_{Cm} \geq a/(1 - U'_0).$$

By substituting (19) in (17) it is obtained:

$$I'_0 \geq 2\nu a / \pi(1 - U'_0) \qquad (20)$$

Equation (20) allows for drawing the border line, after which the conditions for switching the transistors on at zero voltage are broken and the converter stops. The border of the natural commutation can be drawn in the plane of the output characteristics of the converter $I'_0 = f(U'_0, \nu)$. The equation of the output characteristics is known from [3, 4]:

$$\left(U'_0 \sin\frac{\pi}{2\nu}\right)^2 + \left[\left(\frac{\pi}{2\nu} \cdot I'_0 + 1\right)\cos\frac{\pi}{2\nu}\right]^2 = 1 \qquad (21)$$

A family of output characteristics of the converter is shown in fig.4, together with two border lines – at a=0,1 and a=0,02. It can be seen that the bigger the capacity of the snubbers, the bigger the limitations in the output characteristics. It causes difficulties in the operation of the converter with high-ohm loads (close to the real idle running mode). The increase in the snubbers, however, leads to a decrease in the commutation losses in the transistors as well as to limiting the electromagnetic interferences of the converter.

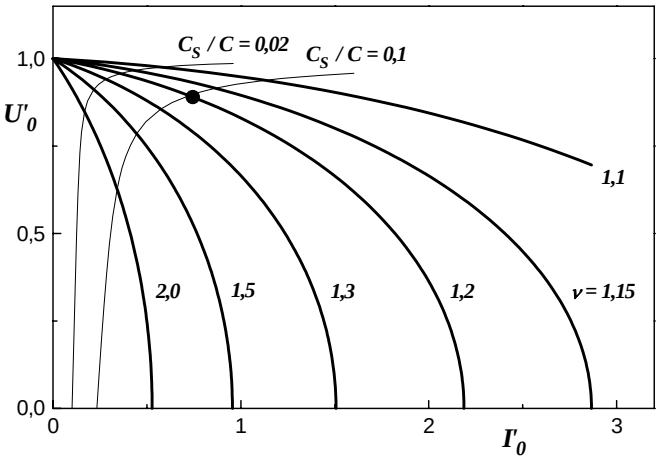

Fig.4. Output characteristics of the converter

III. Simulation Results

Following a methodology, known from [1] and [3], a transistor resonant DC/DC converter has been designed, working at frequencies, higher than its resonant one at these input data: P = 3 kW; f = 100 kHz; U_d =300 V. For the nominal mode of work it has been chosen that ν = 1,15. The values of the elements in the resonant circuit are as it follows: C =46,157 nF, L =72,577 μH. In order to prove the obtained theoretical results the coefficients a=0,1 and k=1, have been chosen, which corresponds to the values $C_1 \div C_4$=4,6157 nF.

The model of computer simulation by means of the software package OrCAD PSpice is shown in fig. 5. Individual schemes for controlling the transistors $Q_1 \div Q_4$ have been introduced. These schemes supply controlling voltage to the gate of the corresponding transistor if at the input of the individual scheme there is a controlling signal and the voltage drain-source of the transistor is practically equal to zero (ZVS).

Computer simulation at ν=1,2 and load resistance R_T=41 Ω has been realized. Fig.6 illustrates the voltage on the transistor Q_4 – V(Q_4:d, Q_4:s), its controlling voltage - V(Q_4:g, Q_4:s), as well as the current in the resonant circuit - I(L).

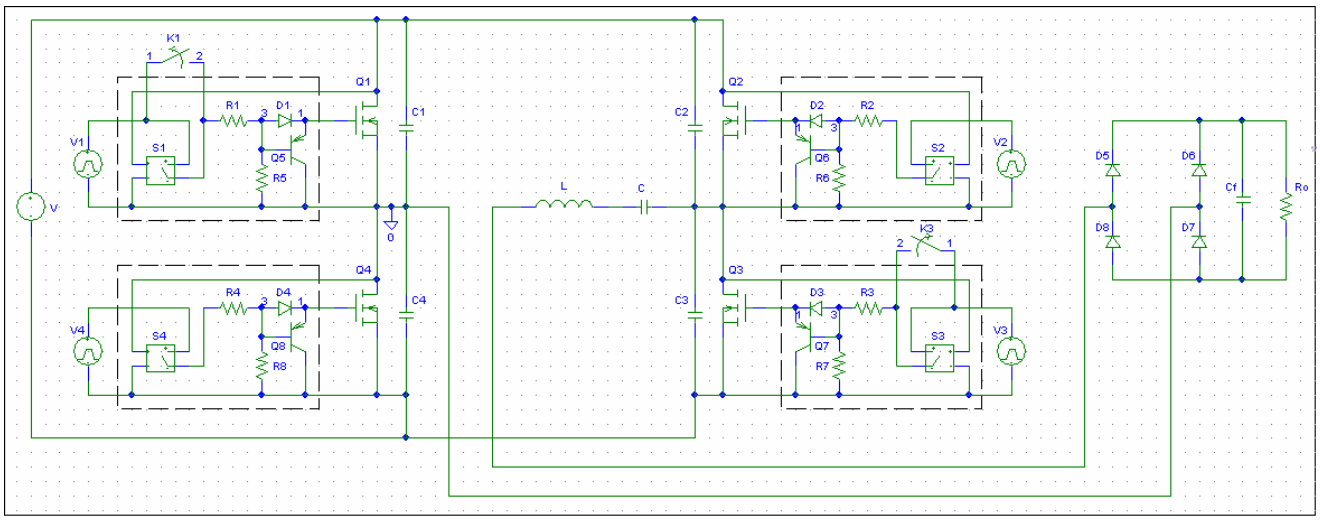

Fig. 5. Computer model of the DC/DC converter

It can be seen that the protective capacitor C_4, connected in parallel to Q_4 does not manage to discharge from $+U_d$ to 0 before the current in the oscillating circuit becomes zero. Then the individual controlling scheme does not supply controlling voltage to the gate of Q_4 and the converter stops working. Fig. 6 shows the failure of commutation which corresponds to the crossing point of the output characteristic at ν=1,2 and the border line at a=0,1 (fig.4).

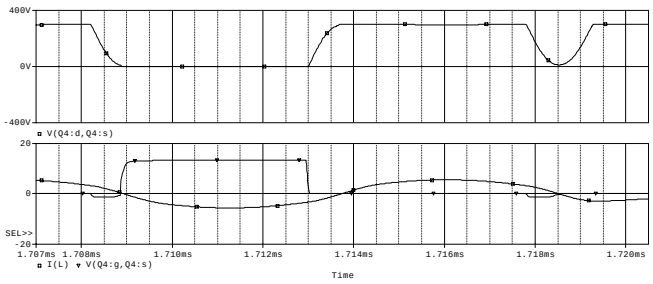

Fig. 6. Result from the simulation of the converter

IV. Conclusions

Analysis of a transistor resonant DC/DC converter working at frequencies, higher than its resonant one, has been carried out by the method of the phase plane. During the analysis the influence of the protective capacitors (snubbers), connected in parallel to the transistors, has been taken into consideration. Equation of the border line after which the conditions for switching the transistors on at zero voltage (ZVS) are broken, has been obtained. The border line of the natural commutation has been drawn in the plane of the output characteristics of the converter. The obtained results can be used in designing wide range of power supply sources for the needs of the electrical power technologies.

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