Simulation of Bulk Traps Influence on the Electrical Characteristics of VDMOS Transistor

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Abstract – **The influence of donor-like and acceptor-like bulk traps on electrical characteristics of VDMOS transistor under high electric field stress is investigated. First, the mechanisms responsible for bulk traps generation are described and the simulation model incorporated into the Silvaco TCAD software package software that takes into account the impact of bulk traps on the device electrical characteristics is given. In addition the process of sample preparation, measurement techniques and measured initial and after-stress electrical characteristics of VDMOS transistor IRF510 are presented. Finally, the influence of bulk defects simulation model parameters on the electrical characteristics is considered using Silvaco simulation tools. It is shown that bulk defects significantly affect on the device behaviour, but they are not the only mechanism responsible for the degradation of electrical characteristics of VDMOS transistor due to high electric field stress.**

Keywords – **Donor-like, acceptor-like, bulk trap, Silvaco.**

I. INTRODUCTION

Over the past six decades, high-speed and low power integrated circuits (IC) are used so widely, permeating every aspect of human life. Accordingly, high-quality circuit design is one of the most critical parts of this technology. Reducing in transistors size continually complicates the device physics and makes device modeling more sophisticated. Because of that, complete fabrication process flow and device electrical characteristics simulation programs, as well as the electronic circuit simulators are the essential tools in the procedure of ICs design.

The electrical instability of MOSFETs is usually associated with hot-carrier trapping in the oxide-semiconductor interface. In the last 30th years, so many investigation reports an experiments which determine the mechanisms leading to device degradation and propose the physical models for the instability explanations [1-3]. In most of these models, the -- presence of defects in semiconductor substrates was neglected, even though the bulk defects may significantly affect on the device electrical characteristics. As it is well known, by using the process and device simulators in the IC design procedure we have the possibility to separate the influence of different parameters, models and mechanisms on the device electrical characteristics. This ability is utilized in this paper to separate bulk and interface trap generation mechanisms due to high electric field stress (HEFS) and simulate and discuss only the bulk traps impact on the device electrical characteristics.

In order to isolate only the bulk trap generation mechanisms due to HEFS on the n-channel power VDMOS electrical characteristics (threshold voltage, transconductance, etc.), it was necessary to simulate its complete technological production process flow. After the procedure of process flow reverse engineering, the doping profile distributions in the simulation domain is obtained by using the process simulator ATHENA [4] which is an integral part of Silvaco TCAD software package. The electrical characteristics of VDMOS transistors and the influence of bulk trap generation mechanisms are simulated by using the device simulator ATLAS [5]. Comparing the obtained simulation results and measured electrical characteristics it is shown that bulk defects significantly affect on the device behaviour, but they are not the only mechanism responsible for the degradation of VDMOS electrical characteristics due to high electric field stress.

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II. BULK TRAPS

A. Bulk Traps Generation Mechanism

The presence of defect centers, or traps, in semiconductor substrates may significantly influence on the electrical characteristics of the device. Trap centers, whose associated energy lies in the forbidden gap, exchange charge with the conduction and valence band through the emission and capture of electrons. The trap centers influence the density of space charge in semiconductor bulk and the recombination statistics.

The donor-like hole trap (**DT**) can be either positive (ionized) when empty or neutral when filed with electron. An empty **DT**, which is positive, can capture an electron or emit hole, while a filled **DT**, which is neutral, can emit an electron or capture hole. Unlike donors, the energy levels for **DT** usually lie in energy gap near the valence band. An acceptor-like electron trap (**AT**) is neutral when empty and negatively charged (ionized) when filled with an electron. A filled **AT** can emit an electron or capture a hole, while an empty **AT** can capture an electron or emit a hole. Likewise, the energy levels for **AT** lie near the conduction band.

B. Bulk Traps Simulation Model

The net charge due to the presence of traps in semiconductor bulk is added on the right hand side of Poisson's equation. The total charge value is defined as:

$$Q_T = q(N_{tD}^{+} - N_{tA}^{-}) = Q_{tD}^{+} - Q_{tA}^{-}, \qquad (1)$$

where N_{tD}^{+} and N_{tD}^{+} are the densities of ionized donor-like and acceptor-like traps, respectively. The ionized density is equal to the product of the donor (*NTD)* and acceptor (*NTA*)

trap densities and its probability of ionization F_{tD} and F_{tA}. The probability of ionization assumes that the capture cross sections are the constant for all energies in a given band, and follows the analysis developed by Simmons and Taylor [6]:

$$F_{tD} = \frac{v_p SIGP \cdot p + e_{nD}}{v_n SIGN \cdot n + v_p SIGP \cdot p + e_{nD} + e_{pD}} \quad (2)$$

$$F_{tA} = \frac{v_n SIGN \cdot n + e_{pA}}{v_n SIGN \cdot n + u_p SIGP \cdot p + e_{nA} + e_{pA}} \quad (3)$$

SIGN and *SIGP* are the carrier capture cross sections for electrons and holes, respectively, υ_n and υ_p are the thermal velocities for electron and holes, while the electron and hole emission rates are defined by:

$$e_{nD} = \frac{1}{DEGEN.FAC} v_n \cdot SIGN \cdot n_i \cdot \exp\frac{E_t - E_i}{kT_L} \quad (4)$$

$$e_{pA} = DEGEN.FAC \cdot v_p \cdot SIGP \cdot n_i \cdot \exp\frac{E_i - E_t}{kT_L} \quad (5)$$

E_i is the intrinsic Fermi level position, E_t is the energy of the discrete trap level defined in relation to valence and conduction band edge for donor and acceptor trap, respectively, T_L is the lattice temperature and *DEGEN.FAC* is the degeneracy factor of the trap center.
In the case where the *k* donor and/or *m* acceptor trap energy levels are defined, the total charges are:

$$Q_{tD}^{+} = q\sum_{\alpha=1}^{k} N_{tD\alpha}^{+} = q\sum_{\alpha=1}^{k} NTD_{\alpha} \cdot F_{tD}^{\alpha} \quad (6)$$

$$Q_{tA}^{+} = q\sum_{\beta=1}^{m} N_{tA\beta}^{-} = q\sum_{\beta=1}^{m} NTA_{\beta} \cdot F_{tA}^{\beta} \quad (7)$$

III. Experimental Procedure

A. Sample Preparation

The devices used in the experiment were power n-channel VDMOS transistor IRF510 (TO-220), with 860 hexagonal cells, is fabricated using conventional Si-gate technology with 10Ωcm p-type <100> oriented substrate. The nominal gate oxide is 120nm thickness grown in dry oxygen ambient and annealed for 20 min in nitrogen at 1100°C. The structure of the device is shown in fabrication technology has been described in more detail in Ref. [14]. It is important to note that the current flows horizontally from the N^+ source through p-channel and then vertically through the N^- epitaxial layer to the bottom drain contact.

The HEFS was performed with the gate biases of V_{GS} = +80 V or V_{GS} = −80 V (source and drain grounded) at room temperature. The gate bias was sufficient to induce significant defect densities in the SiO_2 and at the Si/SiO_2 interface during the total stress time of 150 min. Namely, the electric field in the oxide (about 8 MV/cm) was sufficient to cause Fowler-Nordeheim tunneling of electrons into the oxide either from the silicon substrate (positive V_{GS}) or from the gate (negative V_{GS}). After the HEFS, the transistors were annealed in air at 150 °C with annealing gate bias V_{Ga} = +10 V (source and drain grounded), using the Heraeus HEP2 system of temperature chambers. In order to investigate details of defect kinetics during the repeated stress (e.g. whether some processes reach saturation during the second stress cycle), after about 3000 h of annealing time both the HEFS and thermal post-HEFS annealing were repeated under the identical experimental conditions.

B. Measurement Techniques

The equipment used for the high electric field stressing and electrical characterization consisted of Keithley 237 source-measure unit, Keithley 2400 SourceMeter, and HP8116A function generator. The HEFS and all electrical measurements were performed at room temperature and were completely automated and controlled by a PC.

Two substantially different techniques were used to determine densities of stress-induced defects in the SiO_2 and Si/SiO_2 interface – subthreshold-midgap (MG) method and charge-pumping (CP). The MG method as originally proposed uses analysis of transistor subthreshold I–V curves to determine densities of the oxide-trapped charge and interface traps created during stress and post-stress annealing. The CP technique, in our case modified for use in power VDMOSFETs uses measurements of charge-pumping current to determine number of interface traps; the technique cannot be used to reliably estimate oxide-trapped charge contribution. The CP measurements were performed with source and drain grounded, and triangular gate pulses (frequency 1 MHz, amplitude 4 V) applied to the gate.

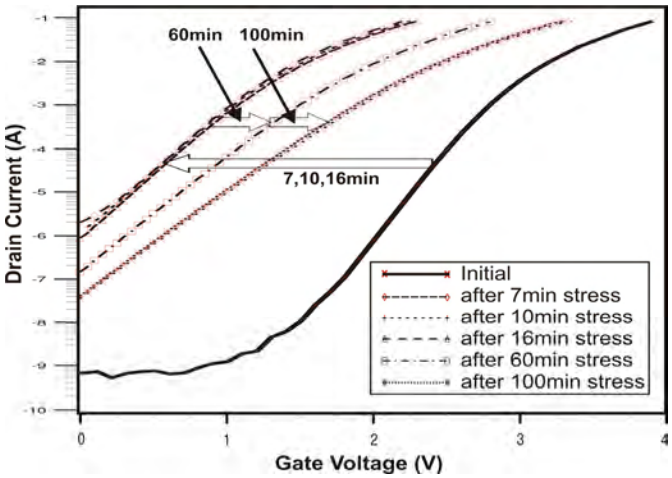

Fig. 1. The measured static electrical characteristics of VDMOS transistor before and after positive gate voltage stress.

From the measured electrical characteristics (Fig. 1) the significant transconductance degradation and subthreshold leak current increase are obvious, while the threshold voltage decreases initially and then returns to increase.

IV. Simulation Results

A. Reverse Engineering of VDMOS Production Flow

In order to simulate the influence of bulk traps formed under the influence of high electric fields, on the electrical characteristics of VDMOS transistor, it is necessary to simulate its complete technological production flow and determine the doping profiles in the simulation domain. This is a very serious problem given the fact that the VDMOS transistor production flow has more than one hundred process steps, whereby each process has dozens of process parameters that are unknown to us.

The initial data known at the beginning of the simulation procedure are the measured electrical characteristics of VDMOS transistors (threshold voltage V_T, output characteristics $I_D=f(V_{DS})$ and transport characteristic $I_D=f(V_{GS},V_{DS}=100mV)$) and basic information about the technology used for its development (type of the technology and the order of process steps). By using these data the manufacturing process flow of VDMOS transistor is reconstructed, and the values of the process parameters (implantation energies and doses, time, temperature and ambient of diffusion processes, etc.) as well as device geometry parameters are determined. After that it was possible to simulate the complete process flow using the process simulator ATHENA that is an integral part of the Silvaco TCAD software package.

The impurities profile distribution is then used as input parameter for simulation of VDMOS electrical characteristics using device simulator ATLAS, which is also a part of the aforementioned TCAD software package.

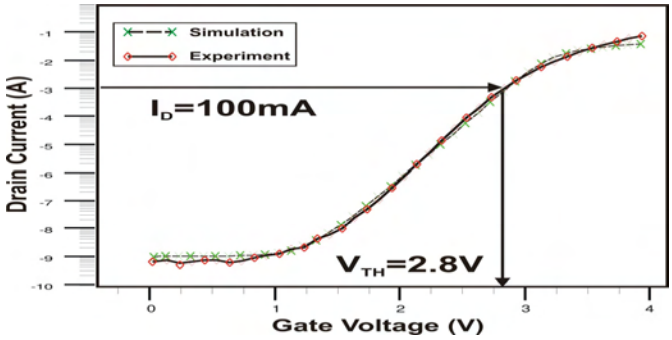

Fig. 2. Comparison of simulation results with the initial measured electrical characteristics of VDMOS transistors after device simulator ATLAS calibration.

B. Silvaco TCAD Software Package Calibration

The next very important step in the simulation of electrical characteristics of power VDMOS transistor is the calibration of device simulator ATLAS. This means that it is necessary to further fine-tuning parameters, which largely depend on the specific technology characteristics, such as: fixed oxide charge density applied at the Si/SiO_2 interface (QF), low-field electron and hole mobility (MUN, MUP), electron and hole velocity saturation (VSATN, VSATP), and electron and hale surface recombination velocities (S.N, S.P). After setting these parameters, a very good agreement of simulation results with the measured initial (unstressed) electrical characteristics of VDMOS transistor is obtained, as shown in Fig. 2.

C. Trends Caused by Vvarying Bulk Trap Ddistribution Parameters

In order to activate bulk traps in ATLAS device simulation tool and to analyze their impact on electrical characteristics of VDMOS transistor the command TRAP is used. TRAP activates donor and/or acceptor bulk traps at discrete levels within the bandgap of the semiconductor and set their parameter values:

TRAP DONOR/ACCEPTOR E.LEVEL=<r>, DENSITY=<r>, DEGEN.FAC=<r>, <capture parameters>

Parameter DONOR/ACCEPTOR specifies donor- or acceptor-type trap levels, DENSITY sets the maximum defect density states of the trap level, while DEGEN.FAC specifies the degeneracy factor of the trap level used to calculate the density. E.LEVEL sets the energy of the discrete trap level. For donors E.LEVEL value is relative to the valence band edge, while for acceptors it depends on the conduction band edge. Capture parameters specifies cross sections of the trap for electrons and holes or their lifetimes in the trap level.

Before trying to match measured electrical characteristics of stressed device with the simulation results it is worth to understand trends caused by varying the bulk trap parameters on the threshold voltage shift, the transconductance degradation and the subthreshold leakage current. The influence of maximum donor-type bulk traps and bulk trap energy level for DD=2.E16 and DD=1.E17 on the VDMOS electrical characteristics are shown on Figs. 3-5, respectively. It is obvious that the threshold voltage decreases when the the maximum concentration of donor-like bulk trap increase. On the other hand, when the donor trap energy level approaches to the bottom of conduction band edge the threshold voltage continue to decrease, while the effects of the transconductance degradation and the subthreshold leakage current increasing are more emphasized.

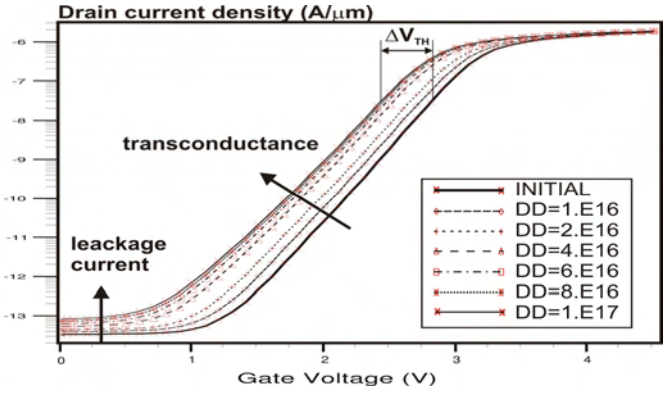

Fig. 3. The influence of maximum density donor-type bulk trap on VDMOS electrical characteristics

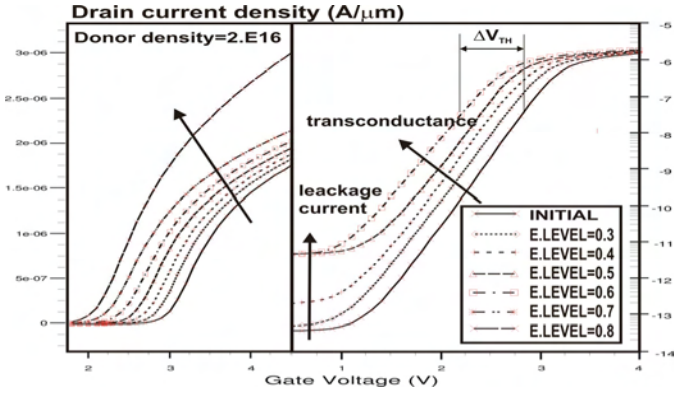

Fig. 4. The influence of donor-type bulk trap energy level on VDMOS electrical characteristics for donor density DD=2.E16

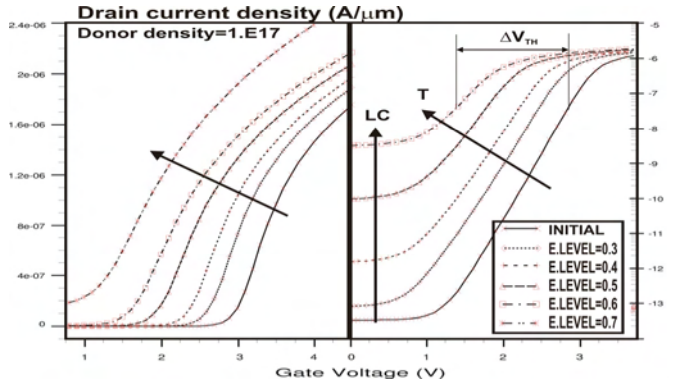

Fig. 5. The influence of donor-type bulk trap energy level on VDMOS electrical characteristics for donor density DD=1.E17

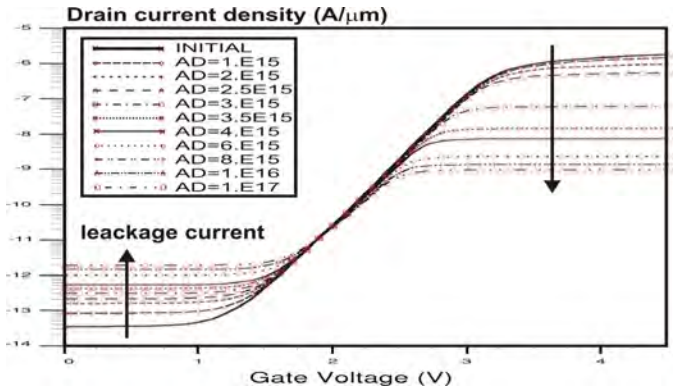

Fig. 6. The influence of maximum density acceptor-type bulk trap on VDMOS electrical characteristics

The influence of maximum density acceptor-type bulk trap on VDMOS electrical characteristics is shown on Fig. 6, and on the basis of their shape, it is clear that the acceptor-like bulk traps are not responsible for the degradation of device characteristics due to positive HFES. Finally, the values of bulk traps distribution parameters and the obtained simulation results are compared with experimentally measured characteristics of stressed VDMOS transistor (Fig. 7). It is important to note that the effects of short-term HFES could not be well simulated when only the influence of bulk traps on characteristics is taken. In that case we have to include in simulation model the influence of donor and acceptor interface traps generation mechanisms. A quite well match with electrical characteristics of longer stressed components can be explained by the fact that the current in these components flows not only through the channel but also vertically through the substrate, where the influence of bulk traps is dominated.

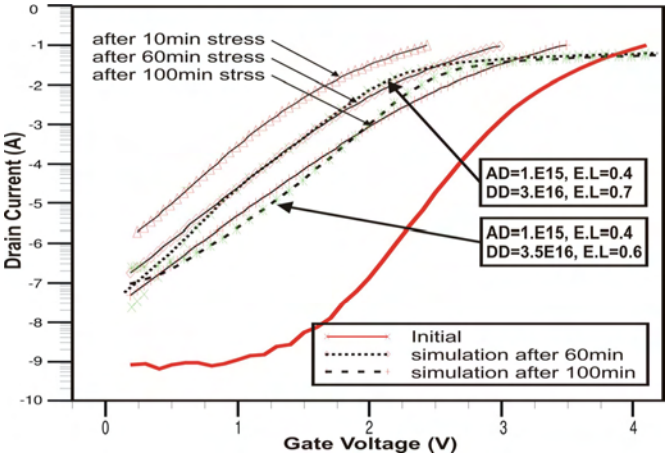

Fig. 7. The comparison of measured and simulated electrical characteristics of stressed VDMOS transistor with values of bulk traps distribution parameters.

V. Conclusion

In this paper the influence of bulk traps on the degradation of electrical characteristics of power VDMOS transistor due to positive HFES is analyzed. It is shown that the degradation effects can be quite good simulated by taking into account only the influence of bulk traps, but for the correct and precise simulation of HFES impact on device characteristics it the necessary to include in the simulation model all relevant effects and generation mechanisms.

Acknowledgement

This work has been partially supported by the Serbian Ministry for Education and Science under the projects TR-33035 and ??.

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