FPAA Implementation of RMS-to-DC Converter for Analog Signal Processing

Ivailo Pandiev[1]

Abstract – **This paper presents a true RMS-to-DC converter employing single Field Programmable Analog Array (FPAA) device. The proposed converter is based on indirect (or implicit) computation method. The conversation circuit consists of a full-wave rectifier, a squarer/divider, low-pass active filter with two external capacitors (averaging circuit) and 8-bit analog-to-digital converter (ADC). The functional elements of the structure are realized by employing available configurable analog modules (CAMs) of the FPAA AN231E04 from Anadigm. The converter has wide-band frequency response and can operate with single supply voltage at 3,3V. Simulation and experimental results show good agreement with theoretical predictions.**

Keywords – **Analog signal processing, Root-mean-square value, Methods of RMS-to-DC conversion, True RMS-to-DC converters, FPAA.**

I. INTRODUCTION

A true Root-Mean-Square (RMS) to DC (RMS-to-DC) converter is a device that provides a dc output voltage, which is proportional to the average energy content in an ac electrical signal. These devices are useful in the fields of instrumentation, communication and medical systems. A variety of RMS-to-DC converters for analog signal processing, are available in the literature [1-7]. In [1] a bipolar RMS-to-DC converter is based on a synthesis of translinear loop squaring/ divider and current-mode low-pass filter. The main drawbacks of this proposed circuit are as follows: first, this circuit operate in only one-quadrant input current; secondly, the circuit is suitable for a voltage supply of more than $5V$. Recently, a new RMS-to-DC converter using translinear-based squarer circuit is proposed [2], where the input current can be a two-quadrant current signal. Because the full-wave rectifier is not required by this conversation scheme, the circuit exhibits a wide bandwidth. However, the implementtation of the circuit is rather complicated and bandwidth is limited to less than $5kHz$. Wider bandwidth ($>100kHz$) is achieved in the converter proposed in [3]. This RMS-to-DC converter is based on the explicit computation method. The circuit can operate with single supply voltage at $2V$ and maximum bandwidth is $60MHz$. Design techniques based on explicit computation of rms value are with limited dynamic range. In [4] is proposed a system based on Discrete Wavelet Packet Transform (DWPT) and Hilbert transform for measuring RMS value and phase angle of the fundamental harmonic of the signal. This system based on DWPT is with great precision and computationally efficient, but it is characterized by a relatively narrow bandwidth (e.g. several tens of Hz).

Many integrated forms of true RMS-to-DC converters have been proposed [5-7]. Most of these ASICs (Application Specific Integrated Circuits) used the implicit method of rms computation employing and absolute value V/I converter, a squarer/divider, low-pass filter, precision current mirror and an output buffer.

While some approaches imply the use of ASICs for the front-end circuits, which requires considerable design time and costs, FPAAs have been recently raised flexible, fast-prototyping and comparatively economical solutions for design of complex analog processing systems [8-10]. To the author's knowledge, an FPAA implementation of a true RMS-to-DC converter has not yet been reported in the literature. It is, therefore, the purpose of this paper to present a voltage-mode RMS-to-DC converter based on implicit computation method.

II. PRINCIPLE OF RMS-TO-DC CONVERTER OPERATION

The definition of the RMS value of an input signal with period of T is given by

$$U_{RMS} = \sqrt{\frac{1}{T}\int_0^T u^2(t)dt}\,, \tag{1}$$

where U_{RMS} is the rms value and $u(t)$ is the instantaneous voltage, a function of time.

Squaring both sides of this equation yields

$$U_{RMS}^2 = \frac{1}{T}\int_0^T u^2(t)dt\,. \tag{2}$$

The integral, given in Eq. (2) can be approximated as an average value

$$Avg\left[u(t)\right]^2 = \frac{1}{T}\int_0^T u^2(t)dt\,. \tag{3}$$

Then Eq. (2) simplifies to

$$U_{RMS}^2 = Avg\left[u(t)\right]^2\,. \tag{4}$$

Dividing both side of Eq. (4) by U_{RMS} yields

$$U_{RMS} = \frac{Avg\left[u(t)\right]^2}{U_{RMS}}\,. \tag{5}$$

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The Eq. (5) provides the basis for the implicit computing method for U_{RMS}. The advantages of implicit rms computation over other methods are fewer components and greater dynamic range. A disadvantage of this method is that it has less bandwidth than either thermal or explicit computation method [5, 11].

Fig. 1 shows the circuit diagram of the voltage-mode true RMS-to-DC converter based on the implicit computation method. The circuit is essentially an analog signal processor that solves Eq. (5). The input stage is an absolute-value circuit that is a precision full-wave rectifier. The output signal $|u(t)|$ of the absolute-value circuit drives the cascade structure of a

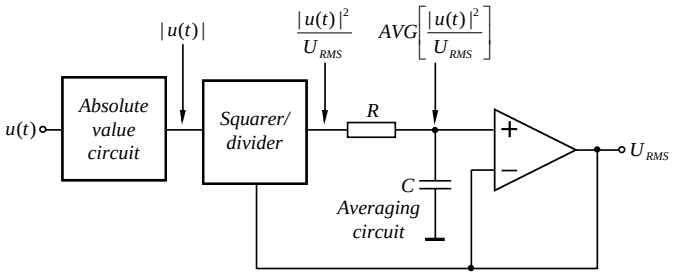

Fig. 1. Circuit diagram of the voltage-mode true RMS-to-DC converter based on implicit computation method.

squarer/driver and a low-pass filter. The squarer/driver squares the signal $|u(t)|$ and divides it by the output signal, which is the average output of the squaring circuit. By closing loop around the divider, Eq. (5) is solved continuously.

III. FPAA for RMS-to-DC Conversion

This section analyzes the suitability of FPAA for RMS-to-DC conversion and conditioning. A subsequent presentation of the Anadigm® FPAA architecture and functionalities [15] allows to link these with those required for conditioning of analog signals with small amplitude and wide bandwidth.

The synthesis of the analog system for RMS-to-DC conversion is strongly conditioned by the incoming signal features, such as amplitude, frequency and noise level. This means that the implementation of the circuit would have to allow changing the gain to cope with a variation in the amplitude of the signal, and it should be able to change the pole frequency of the low-pass filter to different noise levels. These requirements are easily achieved using a FPAA to synthesize this analog system. Moreover, programmable analog arrays offer a tradeoff between performance and system design time. The main drawback presented by the use of FPAAs could be their high power consumption, compared with that of ASICs. This drawback is affordable for implementations that are intended to be a portable instrument.

Among different devices and technologies in the market [12-14], Anadigm offers dynamically programmed Analog Signal Processors (dsASP), in particular the AN231E04 that is a reconfigurable programmable analog device based on switched capacitor (SC) technology. The AN231E04 device consists of a 2×2 matrix of fully Configurable Analog Blocks (CABs), surrounded by programmable interconnect resources and analog input/output cells with active elements. Different circuit configurations with AN231E04 are achieved through manipulation of electronic switches between various circuit components within the CABs. Each CAB contains two operational amplifiers (op amps), Successive Approximation Register (SAR), 8 variable capacitors, and a comparator. The chip has seven configurable input/output structures each can be used as input or output, 4 of the 7 have integrated differrential amplifiers. There is also a single chopper stabilized amplifier that can be used by 3 of the 7 output cells. Each configurable input/output cell contains a collection of resources that allow for high fidelity connections to and from the outside world with no need for additional external components. In order to maximize signal fidelity, all signals routing and processing within the device is fully differential. Accordingly, each input/output cell accepts or sources a differential signal. The AN231E04 devices also contain an 8-bit, 250k samples per second ADC with SAR on the FPAA, thus eliminating the potential need for an external converter.

Programming and testing analog circuits with FPAA ICs can be realized with computer-based development systems, available from the manufacturers. Such development systems include specialized *evaluation printed circuit boards* with FPAA IC sockets and the *AnadigmDesigner2* ECAD system. The ECAD system *AnadigmDesigner2* has the functionality for creating electronic circuits employing CAMs, which map onto portions of CABs, simulation testing of the resulting circuits and programming real FPAA ICs.

IV. FPAA Configuration for RMS-to-DC Conversion

Once the FPAA features have been presented, this section is focused the key qualities and elements of this device that will be used for RMS-to-DC conversion of analog signals. Moreover, the functional circuit of voltage-mode true RMS-to-DC converter based on FPAA AN231E04 is presented.

A. Interfacing of Analog Signals to the FPAA AN231E04

The FPAA AN231E04 uses analog signals that are referenced to $VMR = +1{,}5V$ (Voltage Mid-Rail − VMR) and are limited to the range from 0 to $+3{,}3V$. In Fig. 2 are shown the op amp circuits for interfacing of single-ended signals to the FPAA [16]. The single-ended input signals can be level-shifted to $+1{,}5V$ with non-inverting amplifier stage referenced to $+1{,}5V$.This circuit can also be used to attenuate large signals or amplify small signals. The transfer function of the input stage is given by

$$U_{IN,FPAA} = (R_F / R_N)u(t) + VMR\,, \qquad (6)$$

where $R_P = R_N$.

It is recommended to keep the sum of R_F and $R_P = R_N$ to approximately $100k\Omega$.

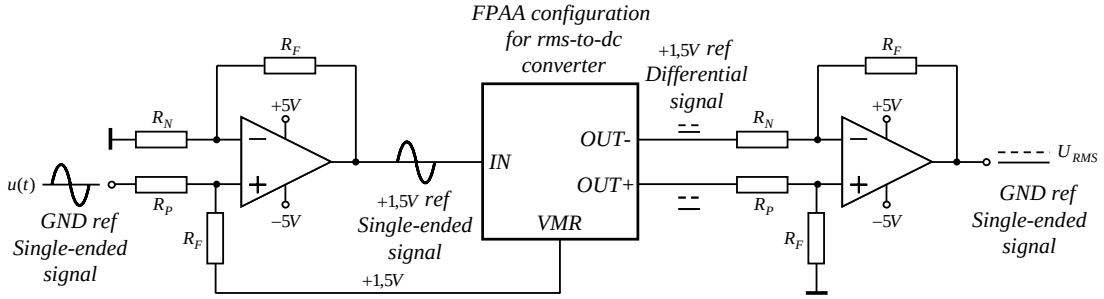

Fig. 2. Op amps circuits for interfacing analog signals to the FPAA device.

The output differential stage is used to level-shift the FPAA output signal and do a differential to single-ended conversion. Furthermore, the output stage can drive external devices with low input impedance and can be used to amplify the FPAA output voltage by any desired amount. For $R_P = R_N$ the transfer function of the output stage can be written as

$$U_{RMS} = (R_F / R_N)(U^{+}_{OUT,FPAA} - U^{-}_{OUT,FPAA}) . \qquad (7)$$

The advantages of the circuit shown in Fig. 3 are that dc information is not lost, signals of any amplitude or dc bias can be handled, and output signal can drive external devices with low input impedance. Also the FPAA output signal can both level-shifted and converted from differential to single-ended.

B. FPAA CAMs for RMS-to-DC Conversion

The RMS-to-DC converter is built by selecting among the available CAMs, shown in Table 1. The *RectifierFilter1* with low-pass filter rectifies an input signal $u(t)$ of either polarity in a manner determined by the other options. A sample input and output waveform is shown on the symbol. The switching clock for this module is set to $250kHz$. This is the highest frequency that allows setting the filter corner frequency to $25kHz$. The *Multiplier1* and *Divider1* square the signal $|u(t)|$ and divide it by the output voltage. The output signal of the squarer/driver is a product of two input voltages with multiplication and divisor factor equal to 1. The output low-pass filter that eliminates noise components over several mHz is developed using *FilterLowFreqBilinear2* with external capacitors C_{AV1} and C_{AV2}. Finally ADC produces an 8-bit digital output word proportional to the U_{RMS}.

C. FPAA Cconfiguration of RMS-to-DC Converter

By placing and routing presented above CAMs in the software interface is created a functional circuit. FPAA configuration of RMS-to-DC converter that solves Eq. (5) is shown in Fig. 3. The differential input voltage is connected to the FPAA input cell 2 (pins 09 and 08). In bypass mode, the input signals are routed directly through the cell, bypassing all active circuit elements. The output differential voltage is obtained by the output cell 6 (pins 17 and 18). In bypass mode, the cell's output pins are being driven directly by the low-pass filter connected to the output cell. The digital signals by ADC "Synch" and "Data" are routed to the upper and lower pins of the output cell 7 (pins 19 and 20). Each data bit will become valid during the SAR clock period Clock B (from pin 42). The external averaging capacitors C_{AV1} and C_{AV2}, connected between nodes *n7* and *n9* are chosen with values equal to $1{,}2\mu F$.

V. Simulation and Experimental Results

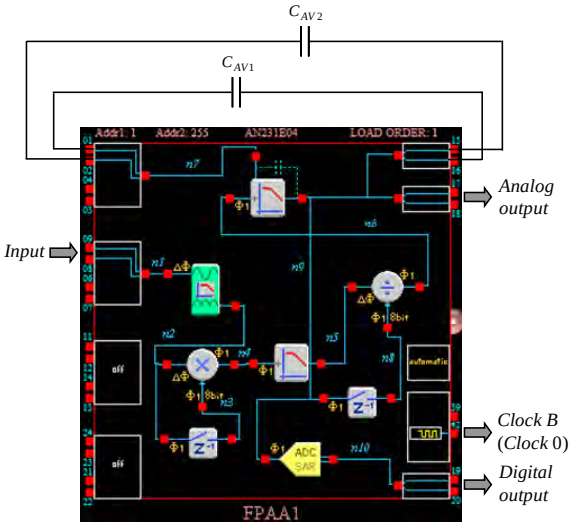

Fig. 3. FPAA configuration of RMS-to-DC converter from Fig. 1.

The workability of the proposed RMS-to-DC converter of Fig. 3 is presented through the simulation results using the simulator built in *AnadigmDesigner2* and also through the experimental results from the circuit configured on prototype board. The experimental test that has been used for validating the FPAA configuration is based on the AN231K04-DVLP3 – Development Board [17]. The AN231K04-DVLP3 is built around the AN231E04 device, biased with $+3{,}3V$ supplies. In Table 2 are presented the experimental results for the performance of the FPAA-based circuit shown in Fig. 3. The maximum error is not greater than 0,5% for the basic waveforms. The tests are performed for input signal with peak value of $1{,}5V$ and frequency $1kHz$. The bandwidth of the circuit is $20kHz$ at $1V$rms input. The high-frequency response is limited by stray capacitance in the circuit board and the finite bandwidth of the *RectifierFilter1*.

TABLE I
FPAA CAMS FOR RMS-TO-DC CONVERSION

Name		Options	Parameters	Clocks
RectifierFilter1		Rectification: full wave Polarity: non-inverting	Corner frequency [kHz]: 25 Gain: 1,00	Clock A: 250kHz (Clock 3)
Multiplier1		Sample and hold: off	Multiplication factor: 1,00	Clock A: 250kHz (Clock 3) Clock B: 4000kHz (Clock 0)
Hold 1 (2)		Input sampling phase: phase1	none	Clock A: 250kHz (Clock 3)
FilterBilinear1		Filter type: low-pass Resource usage: min. resources	Corner frequency [kHz]: 25 Gain: 1,00	Clock A: 250kHz (Clock 3)
Divider1		Sample and hold: off	Divisor factor: 1,00	Clock A: 250kHz (Clock 3) Clock B: 4000kHz (Clock 0)
FilterLowFreqBilinear2		Independent variable: Corner frequency Polarity: non-inverting	Corner frequency [mHz]: 20 Gain: 1,00 External cap value [μF]: 1,2	Clock A: 250kHz (Clock 3)
ADC-SAR1		Input phase: phase1	none	Clock A: 250kHz (Clock 3) Clock B: 4000kHz (Clock 0)

TABLE II
EXPERIMENTAL RESULTS OF THE CIRCUIT IN FIG. 3

Power requirements	
Supply voltage	$+3{,}3V_{DC}$
Power	$166mW \pm 50mW$
Input characteristic	
Input voltage	$1V\ rms$
Bandwidth of the input signal	$20kHz$
Input resistance	$\approx 10M\Omega$
Accuracy	
Crest factor ($CF = U_{PEAK} / U_{RMS}$):	
$CF = \sqrt{2}$ (undistorted sine wave),	error 0,5% ;
$CF = \sqrt{3}$ (triangle wave),	error 0,45%;
CF=1 (symmetrical square wave),	error 0,5%.

VI. CONCLUSION

In this paper a true RMS-to-DC converter trough the use of an implicit computation method has been proposed. The conversation circuit consists of a full-wave rectifier, a squarer/ divider, low-pass filter with two external capacitors (averaging circuit) and 8-bit ADC. The selected FPAA is an Anadigm AN231E04, where the analog signal processing is implemented. The experimental results, obtained for the various waveforms confirm the results of the theoretical analysis.

ACKNOWLEDGEMENT

This paper is a part of a project which is sponsored by the research program of the Technical University of Sofia, Bulgaria.

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