Behavioral VHDL-AMS Model for Monolithic Voltage-Controlled Amplifier

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Abstract – **This paper presents behavioral VHDL-AMS model for monolithic voltage-controlled amplifier (VCA). The proposed model is independent of actual technical realizations and is based upon compromises regarding the representation of exact circuit structures in the model. For creating the model, simplification and build-up techniques known from macro-modeling operational amplifiers have been adapted. The model accurately reflects input impedance, transfer function (amplifier gain versus control voltage), small-signal frequency response, CMRR versus frequency, large-signal pulse response, output characteristic (voltage and current limitations) and output resistance. Model parameters are extracted for the monolithic voltage-controlled amplifier VCA810 from Texas Instruments as an example. The verification check of the model is performed by comparison of the simulation results with the manufacturer's data and with the results obtained by simulation of the PSpice macro-model supplied from Texas I. To confirm the workability of the proposed VCA model some practical electronically controllable analog circuits are investigated. The basic parameters obtained by simulations are compared with the results of the circuits using a valid PSpice macro-model and theoretically calculated parameters.**

Keywords – **Programmable analog circuits, Voltage-controlled amplifiers, Behavioral models, VHDL-AMS, Mixed-signal simulation.**

I. Introduction

The monolithic voltage controlled amplifiers (VCAs) are basic elements of contemporary analog-digital (mixed) circuits and systems. They have an analog signal input, an analog signal output and a digital control of the voltage amplification. Internally, the VCA is based on voltage-controlled two-quadrant analog multiplier. The gain-control sub-circuit converts the controlling voltage to a current. This current varies the transconductance g_m of the current mirror, which specifies the bias currents of the differential stage. Therefore the bias currents variation alters the transconductance g_m of the differential transistor pair. As a result the voltage gain of the amplifier is modified in the specified range. In addition, the most of the VCAs contain input and output voltage follower [1-3].

Testing the workability of electronic circuits with VCAs is done usually using SPICE (Simulation Program with Integrated Circuit Emphasis) based programs. A variety of SPICE macro-models for the VCAs, is available in the literature [4-8]. The majority of published macro-models contains extensive number of active and passive elements. Furthermore, testing complete mixed-signal systems with large number of elements is an extremely difficult process and may often become infeasible due to the limitation of simulation capacity.

One method to decrease simulation time and improve the convergence, without a significant losses of information, is by using behavioral modeling technique. Nowadays one of the most effective techniques for behavioral modeling of mixed-signal electronic circuits is by using VHDL-AMS. The literature survey reveals that behavioral models for the VCAs have not been available yet. Without any doubt behavioral models for basic types of VCAs are necessary for simulating mixed-signal circuits and systems. The goal of this paper therefore is to develop a behavioral VHDL-AMS model that accurately simulates the basic electrical characteristics of most common VCAs based on two-quadrant analog multiplier.

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II. A Practical Approach to Generate Behavioral Models

In this section is presented a specific practical approach for generation of behavioral models of complex analog and mixed systems. The proposed design approach is based on the methodology for generating behavioral models of A/D systems and a practical approach for managing simulation projects given in [10-12]. The design approach diagram is shown in Fig. 1.

The presented approach has two basic branches. The left

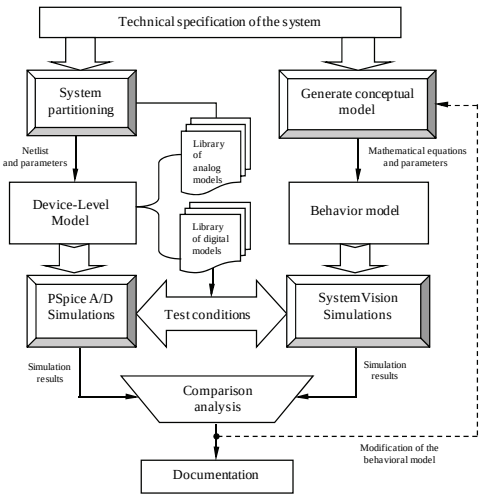

Fig. 1. A practical approach to generate behavioral models.

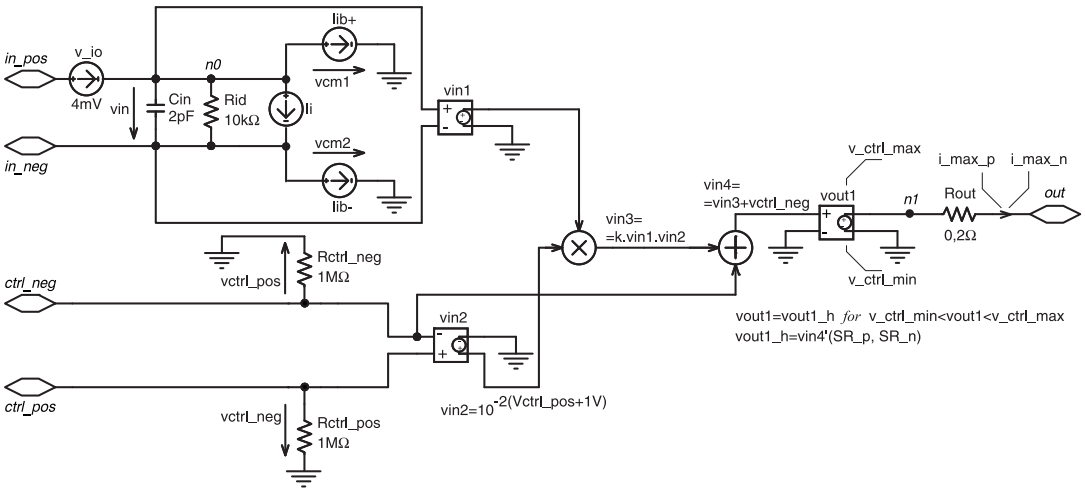

Fig. 2. Circuit diagram for the behavioral voltage-controlled amplifier model.

one is related to generation of a device-level model from actual device and the right one is the procedure for generating the behavioral model. The *device-level model* called *micromodel*, reflects most electrical parameters of the actual device. The *conceptual model* is a mathematical and logical representation of the actual device and the *behavioral computerized model* is the conceptual model implemented on a computer. The conceptual model is developed through an *analysis phase* and the computerized model is developed through a *computer programming* and *implementation phase*.

Once the models are created the comparison analysis is performed. The purpose of comparison analysis is to guarantee the correct behavior of each element in the developed model. In this process each element is tested to ensure that, firstly, they behave in the manner intended by the model code and, secondly, that their behavior is representative of the actual device.

In case the computer model, does not respond fully to the technical specifications, modification and optimization of the structure and the mathematical equations are needed.

Finally, the documentation of the behavioral model should include the conceptual model (critical for the future reuse of the model), a detailed description of the computer model and simulation results for the included electrical parameters.

III. BEHAVIORAL MODELING WITH VHDL-AMS

The technical requirement for effective models is generally agreed when the simplest possible model is developed. Simple models have a number of advantages. They can be developed faster, are more flexible, require less data, run faster and it is easier to interpret the results since the structure of the model is better understood. As the complexity increases, these advantages are lost [10].

The created behavioral model of the VCA is developed following the design approach given in Fig. 1 by using a style combining structural and mathematical description. The structural description is the netlist of the model and the behavioral description consists of simultaneous statements to describe the continuous behavior. An object of research and modeling is a monolithic voltage-controlled amplifier VCA810 from Texas I. [12]. The internal structure of the VCA810 is based on voltage-controlled two-quadrant analog multiplier, which has differential input and single output. The gain control voltage V_c for VCA810 will adjust the gain from $-40dB$ $(0{,}01)$ at $V_c = 0V$ to $+40dB$ (100) at $V_c = -2V$.

The review of the available technical documentation for mixed-signal ICs showed that VCA810 is a typical representative of the base structure used for implementation of controllable amplifiers.

A. A behavioral language: VHDL-AMS

VHDL-AMS is a comparatively new standard 1076.1 of VHDL that supports hierarchical description and simulation of analog, digital and mixed-signal applications with conservative and non-conservative equations [13, 14]. On the mixed-signal side a variety of abstraction levels is supported. The VHDL-AMS modeling is not restricted to mixed-signal applications but also supports thermal and mechatronic systems.

B. A voltage-controlled amp behavioral VHDL-AMS model

The proposed model of the VCA is built using the results obtained by analyses of the SPICE based macro-model for VCA in [8] and by using the results for the behavioral models presented in [9]. The circuit diagram of the VCA behavioral model is shown in Fig. 2, where the different stages are presented with controlled sources and passive RC components. The model includes the following elements and parameters with numerical values: $r_{id} = 10k\Omega$ and $c_{in} = 2\,pF$ – input resistance and capacitance; $V_{io} = 4mV$ – input offset voltage; $I_{io} = 100nA$ – input offset current; $I_{ib} = 6\mu A$ –input bias current; $f_{pi} = \omega_{pi} / 2\pi = 30MHz$ – the $-3dB$ pole frequency; $f_{cm} = 2MHz$ – the $-3dB$ common mode pole frequency; $rctrl\_pos = rctrl\_neg = 1M\Omega$ – positive and negative resistance of the voltage controlled source; $CMRR$ – Common-Mode Rejection Ratio; A_{d0} is differential dc gain and can be defined using equation $A_{d0} = 10^{-2(Vc+1)}$ and A_{cm} is CM gain;

$SR\_p = -SR\_n = 350V/\mu s$ – positive and negative SR; $v\_\sup ply\_p = 3{,}2V$ ($v\_\sup ply\_n = -3{,}2V$) – positive and negative voltage drops for the output voltage

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library IEEE;
use IEEE.MATH_REAL.all;
use IEEE.electrical_systems.all;
entity vca_810 is
     generic (
   --generic parameters here);
   port (terminal in_pos, in_neg, ctrl_pos, ctrl_neg, output, nvdd, nvss :electrical);
end entity vca_810;
architecture default of vca_810 is
   -- inner terminals
   terminal  n0, n1 : electrical;
   -- branch quantities
   quantity v_io across i_io through in_pos to n0;
   quantity vin across iin , icin, ii through n0 to in_neg;
   quantity vdd across nvdd;
   quantity vss across nvss;
   quantity icc through nvdd to ELECTRICAL_REF;
   quantity iee through nvss to ELECTRICAL_REF;
   quantity vcm1 across iib1 through n0 to ELECTRICAL_REF;
   quantity vcm2 across iib2 through in_neg to ELECTRICAL_REF;
   quantity vctrl_pos across ictrl_pos through ctrl_pos to ELECTRICAL_REF;
   quantity vctrl_neg across ictrl_neg through ctrl_neg to ELECTRICAL_REF;
   quantity vout1 across iout1 through n1 to ELECTRICAL_REF;
   quantity vrout across irout through n1 to output;
   quantity vout across output to ELECTRICAL_REF;
  -- free quantities
    quantity vin1 : real;
    quantity vin2 : real;
    quantity vin3 : real;
    quantity vin4 : real;
    quantity vcm :voltage;
    quantity vmid :voltage;
    quantity irout_h : current;
    quantity vout1_h : voltage;
  -- constants declarations here
begin
   --***input stage***--
    v_io == vio;
    ii == iio / 2.0;
    iib1 == iib;
    iib2 == iib;
    icc == pos_s_c;
    iee == neg_s_c;
    iin  == vin / rid;
    icin == cin*vin'dot;
    vcm  == ((vcm1+vcm2)/2.0);
    vmid == (vdd+vss)/2.0;
    vin1 == vin'ltf(num_p, den_p) + (1.0/cmrr)*vcm'ltf(num_cm, den_cm) + vmid;
  --***control stage***--
    ictrl_pos  == vctrl_pos / rctrl_pos;
    ictrl_neg  == vctrl_neg / rctrl_neg;
  --gain vs control voltage—
 if vctrl_pos'above(v_ctrl_min)       use  vin2 == 0.0001;
    elsif not vctrl_pos'above(v_ctrl_max)  and vctrl_pos'above(-2.5) use  vin2 == 100.0;
    elsif not vctrl_pos'above(-2.5) use vin2 == 1.0;
    else vin2 == (10.0) ** (-2.0*(vctrl_pos+1.0));
 end use;
  --***intermediate stage***--
    vin3 == k*vin1 * vin2;
    vin4 == vin3 + vctrl_neg;
  --***output stage***--
    vout1_h == vin4'slew(SR_p,SR_n);
    irout_h == vrout/rout;
 if vout1_h'above(vdd - v_supply_p)         use  vout1 == vdd - v_supply_p;
   elsif not vout1_h'above(vss - v_supply_n) use  vout1 == vss - v_supply_n;
   else vout1 == vout1_h;
 end use;
 if irout_h'above(i_max_p) use   irout == i_max_p;
  elsif not irout_h'above(i_max_n) use    irout == i_max_n;
  else irout == irout_h;
 end use;
end architecture default;
```

Fig. 3. A VCA behavioural VHDL-AMS model.

limitation; $i\_\max\_p = -i\_\max\_n = 60mA$ – maximum output currents; $r_{out} = 0{,}2\Omega$ – output resistance.

The proposed model includes small- and large-signal effects such as (1) input impedance, (2) transfer function (amplifier gain versus control voltage), (3) small-signal frequency response, (4) CMRR versus frequency, (5) large-signal pulse response, (6) output characteristic (voltage and current limitations) and (7) output resistance. The mathematical equations that describe the model can be given as

$$i_{in} = v_{in}\left(\frac{1}{r_{id}} + sc_{in}\right) \tag{1}$$

$$v_{cm} = (v_{cm1} + v_{cm2})/2 \tag{2}$$

$$v_{mid} = (v_{ss} + v_{dd})/2 \tag{3}$$

$$v_{in1} = \frac{\omega_p}{s+\omega_p} v_{in} + \frac{1}{CMRR} v_{cm} \frac{s+\omega_{cm}}{\omega_{cm}} + v_{mid} \tag{4}$$

$$i_{ctrl\_pos} = v_{ctrl\_pos} / r_{ctrl\_pos} \tag{5}$$

$$i_{ctrl\_neg} = v_{ctrl\_neg} / r_{ctrl\_neg} \tag{6}$$

$$v_{in2} = \begin{cases} 0{,}0001, & v_{ctrl\_pos} > 0{,}15V \\ 10^{-2(v_{ctrl\_pos}+1)}, & -2V < v_{ctrl\_pos} < 0{,}15V \\ 100, & -2{,}5V < v_{ctrl\_pos} < -2V \\ 1, & v_{ctrl\_pos} < -2{,}5V \end{cases} \tag{7}$$

$$v_{in3} = k v_{in1}.v_{in2} \tag{8}$$

$$v_{in4} = v_{in3} + v_{ctrl\_neg} \tag{9}$$

$$SR = dv_{in4}/dt \tag{10}$$

$$v_{out1\_h} = v_{in4} \tag{11}$$

(12)

$$v_o = \begin{cases} v_{dd} - v\_\sup ply\_p - i_{rout\_h}.r_{out}, & v_{in4} \geq v_{dd} - v\_\sup ply\_p \\ v_{in4} - i_{rout\_h}.r_{out}, & v_{dd} - v\_\sup ply\_p < v_{in4} < v_{ss} - v\_\sup ply\_n \\ v_{ss} - v_{\sup ply\_n} - i_{rout\_h}.r_{out}, & v_{in4} \leq v_{ss} - v_{\sup ply\_n} \end{cases}$$

Fig. 3 shows the behavioral VHDL-AMS model of VCA. Library clause and the use clause make all declarations in the packages math_real and electrical_systems visible in the model. This is necessary because the model uses nature electrical and constant math_2_pi for the value of 2π from packages. The proposed model is composed by an e*ntity* and an *architecture*, where bold text indicates reserved words and upper-case text indicates predefined concepts. The entity declares the generic model parameters and specifies seven interface terminals of nature electrical. The proposed model includes the following electrical terminals: in_neg, in_pos – inverting and non-inverting inputs, ctrl_neg, ctrl_pos – inverting and non-inverting inputs of the voltage-controlled source, output – output, nvdd, nvss – positive and negative supply voltage

terminals. Furthermore, the model has two inner terminals: n0 and n1. They are used to specify the voltages v_io and vout1 respectively.

The architecture is subdivided into four parts according to the functions of the different elements: *input*, *control*, *intermediate* and *output stage*. It contains the implementation of the model. The architecture is coded by using behavioral description that consists simultaneous statements.

IV. Model Performance

The verification of the proposed behavioral model shown in Fig. 3, is performed by comparing simulation results with the manufacturer's data and with the results obtained by simulation of the PSpice macro-model supplied from Texas I. The simulation modeling of the behavioral model was implemented within simulation program SystemVision (from Mentor Graphics). Based on the simulation results, conclusions for value of relative error are made. The value of the average relative error ε_{av} is not higher than 4,5%. Compared with PSpice macro-model, the proposed model is more precise (the average error for the PSpice model is $\approx 15\%$). Moreover, the CMRR vs. frequency and the limitations in transfer function are not included in the PSpice macro-model.

For validation check of the proposed model, simulation of first-order low-pass filter shown in Fig. 4 was carried out for both the aforementioned model and the macro-model given by Texas I. in the PSpice library. The simulation results are shown in Fig. 5 and Fig. 6. Comparison with theoretically calculated parameters (for the pass-band gain and the pole frequency) shows the advantages of the proposed model ($\varepsilon_{av} = 9\%$) over the macro-model ($\varepsilon_{av} = 12\%$).

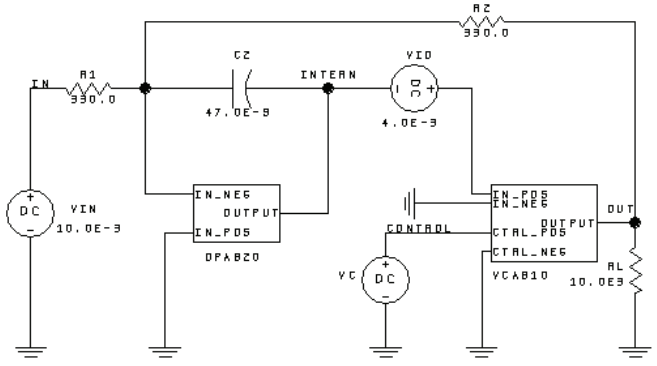

Fig. 4. A VCA behavioral VHDL-AMS model.

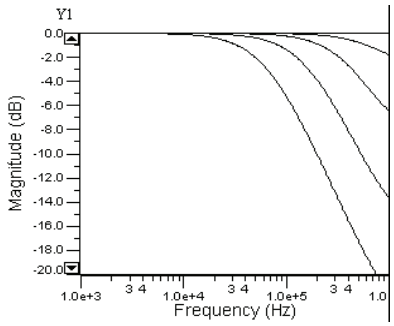

Fig. 5. The simulated response of the low-pass filter shown in Fig. 4 for the proposed VHDL-AMS model.

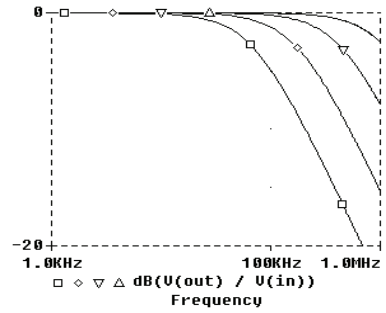

Fig. 6. The simulated response of the low-pass filter shown in Fig. 4 for the VCA810/BB.

V. Conclusion

In this paper a generalized behavioral VHDL-AMS model of monolithic VCA based on two-quadrant analog multiplier has been presented. The proposed model accurately simulates the actual performance of typical VCA for a wide range of frequencies. To achieve simplicity of the mathematical equations describing the model, it neglects several second-order effects found in the VCAs, such as the noise, the temperature effects and the PSRR. The efficiency of the model was proved by comparison between the datasheet parameters of the monolithic controllable amplifier VCA810 and simulation results.

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