Comparative Analysis of the Methods of Defining the Switching Losses in Class D Audio Amplifier – part 1.

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Abstract – **The aim of the proposed article is to make a comparative analysis of the switching losses in power stage Class D amplifiers. This method uses specific parameters of the output stage, whose aim is to define the output efficiency. Out of the numerical experiments we can adequately identify the switching losses of the output stage according to the type of the output transistors. The results obtained in this scientific experiment relate to type Dual N-Channel Enhancement Mode Field Effect Transistor AO4916.**

Keywords – **switching losses, switching frequency**

I. INTRODUCTION

In this article several numerical experiments are conducted to determine the output switching losses in the audio output stage class D. The methods used for analysis and evaluation are based on already known computational methods by which we identify the switching losses in the power stage transistors. These losses are defined by changing the load current. In order to maximize the accuracy of the results several studies have been conducted, such as:

- Numerical experiment to identify the switching losses at various values of the load current;
- Numerical experiment to identify the switching losses at various values of the switching frequency;
- Numerical experiment to identify the switching losses during concomitant modification of the two parameters – load current and switching frequency;
- Comparison of the results for each of the two studies according to known methods for assessment.

II. ANALYSIS OF THE METHODS FOR DETERMINING THE SWITCHING LOSSES

A point of particular interest is the simulated comparison research of the switching losses of two of the known methods [1], [2]. With reference to expression.1, we know that the output losses [5] are defined as the sum of the: switching losses + conduction losses + Gate losses.

$$P_{total} = P_{sw} + P_{cond} + P_{gate} \qquad (1)$$

where: P_{sw} - switching losses; P_{cond} - conduction losses; P_{gate} gate losses.

This means that the switching losses are only one component for defining the complex losses. The comprehensive scientific analysis will show that they can be compared using various methods for assessing the switching losses [3], [4], [5]. In order to determine these losses there are two known methods of assessment. These methods take into account parameters such as: power supply, drain current and conduction resistor. The first published method [5] argues that the value of the switching losses is determined by the expression:

$$P_{sw_1} = C_{oss} \cdot U^2{}_{dd} \cdot f_{sw} + I_d \cdot U_{ds} \cdot t_f \cdot f_{sw} \qquad (2)$$

Another expression extends the analysis and defines the same losses but in the form:

$$P_{sw_2} = [0{,}5.I_d \cdot U_{dd} \cdot (t_r + t_f) \cdot f_{sw}] + \ldots$$
$$\ldots + [0{,}5 \cdot C_{oss} \cdot U^2{}_{dd} \cdot f_{sw}] + \ldots \qquad (3)$$
$$\ldots + [K \cdot 0{,}5 \cdot Q_{rr} \cdot U_{dd} \cdot f_{sw}]$$

where: C_{oss} – output switching capacity; U_{dd} – DC power supply; f_{sw} – switching frequency; I_d – maximum drain current; U_{ds} - maximum drain-source voltage; t_r – rise time to switch on the transistor; t_f – fall time to switch off the transistor; Q_{rr}- reverse ratio output charge; K – static coefficient defined by the working temperature and value of the charge Q_{rr}.

Considering the second expression we realize that the size of the charge Q_{rr} depends on the fast diode connected in parallel between the source-drain (D-S) of the switching transistor. This diode is included in reverse direction to the terminals DS which protect the transistors from reverse voltage. Q_{rr} charge is defined for the time of obstruction of the

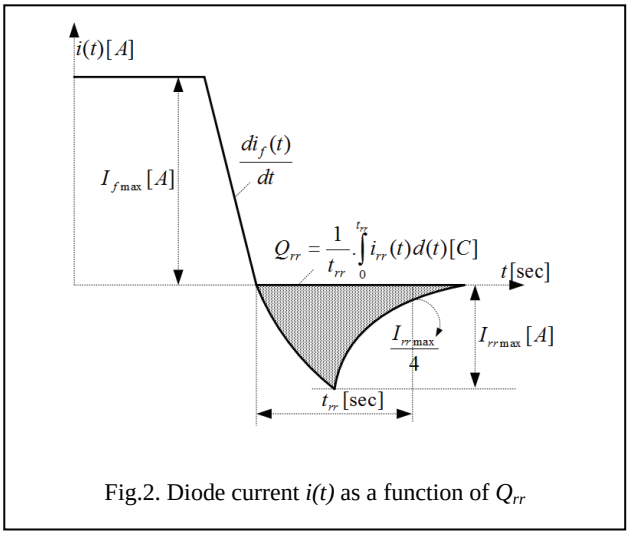

Fig.2. Diode current *i(t)* as a function of Q_{rr}

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diodes t_r - Figure 2, by the expression:

$$Q_{rr} = \frac{1}{t_{rr}} \cdot \int_0^{t_{rr}} i_{rr}(t) \cdot dt \qquad (4)$$

Besides this charge, in the second expression 2, two additional parameters are introduced: coefficient K and reverse ratio output charge Q_{rr}. It is expected that these two parameters will increase the accuracy to identify the switching losses. Whether this is correct or not will be determined after the experiment defining the switching losses when changing any of the participating parameters. To conduct numerical experiments we need to determine the limits of the supply voltage. The magnitude of this voltage is determined by the expression:

$$U_{dd} = 2 \cdot \frac{\sqrt{2 \cdot P_{out} \cdot R_{load}}}{M} + U_{ds_{sat}} \qquad (5)$$

where: P_{out} – is a output power of the stage; R_{load} – load; $M=2,2.\delta=2,2.(ti/T)$ – duty cycle; $Uds_{sat}=(0,1\text{-}0.3)V$

From Eq.5. the maximum supply voltage can be determined. For this reason the first numerical experiment will determine the output voltage modification with change of the output power at constant load R_{load}.

On the other hand carrying out a numerical experiment requires pre-selection of the switching transistors. For the purposes of the scientific experiment we selected parameters for the Dual N-Channel Enhancement Mode Field Effect Transistor AO4916 with base parameters [6]: V_{ds}=30V; I_{dmax}=8.5A(Vgs=10V) $C_{oss}=190pF$; $Q_{rr}=9.2nQ$.

III. NUMERICAL EXPERIMENTS AND DISCUSSION

A. Numerical experiments to define the maximum power supply

To carry out the numerical simulation it is necessary to define the limits of the voltage supply at a constant frequency. This limitation will follow from the maximum parameters of the selected transistor voltage $V_{ds}=30V$, which will determine the maximum output power. This means that exploring the modification of the output voltage will limit the voltage supply $U_{dd}=30V$. We will make examination by conducting the numerical experiment with the following data: $R_{load}=4\Omega$; : $P_{out}=(1\text{-}30)W$; $\delta=(1\text{-}85)\%$ Applying these values to expression 5 we will get the results shown in Fig.3.

From those numerical experiments the maximum permissible value of the supply voltage $U_{dd}=30V$ is obtained at which the maximum output power is limited to the value of $P_{outmax}=15W$.

The resulting value will be used to limit the subsequent experiments. From the output power we will determine the maximum drain current by the expression:

$$I_{d\max} = \frac{2 \cdot P_{out\max}}{U_{dd}} \qquad (6)$$

Replacement the values of output power and supply voltage we obtained:

$$I_{d\max} = \frac{2 \cdot 15}{30} = 1A$$

The maximum value of the $U_{dd}=30V$, $P_{outmax}=15W$ and drain current $I_{dmax}=1A$ will be used to limit the subsequent experiments.

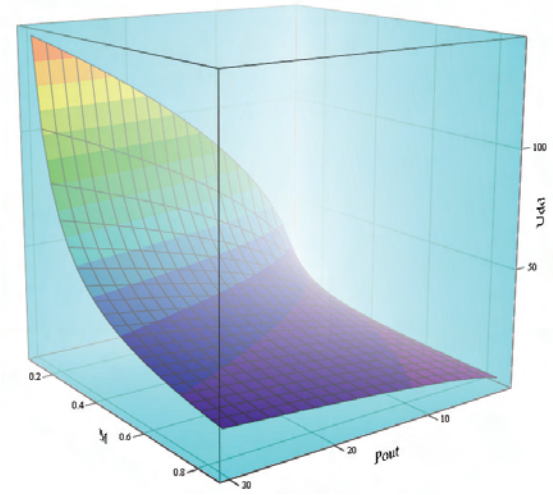

Fig.3. Numerical experiment to define the maximum output power

B. Numerical experiment to define the switching losses with different drain current

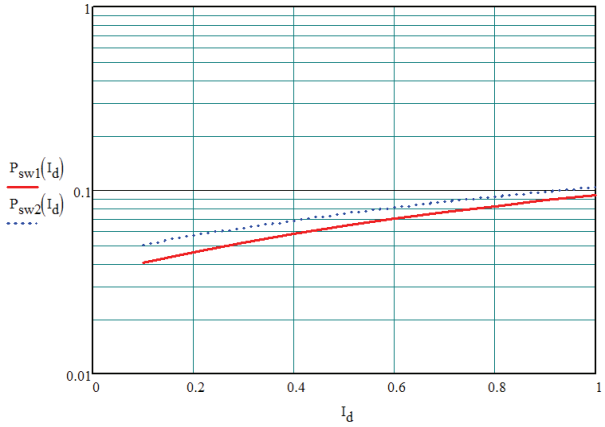

Fig.4. Numerical experiment to define the switching losses P_{sw1} and P_{sw2} with different load current

For the purposes of the scientific experiment, let's keep constant two parameters: the maximum voltage supply $U_{dd}=30V$ and the switching frequency $f_{sw}=200kHz$. Then we will determine the load current modification. The purpose of the program testing is comparison of switching losses P_{sw} on the both known methods (Expression 1 and expression 2) [5] The obtained result is shown in fig.4. In the research area there is a relatively small change of the $P_{sw1.}$ We also notice that the switching losses P_{sw1} remain relatively constant, the equivalent values show a slight discrepancy P_{sw2} resulting from a change of the load current. Additional parameters of the study are $C_{oss}=190pF$; $U_{dd}=30V$; $I_d=0,1\text{-}1A$; $t_r=t_f=10ns$

C. Numerical simulation to identify the switching losses to amend the operating frequency

In this numerical simulation it is necessary to determine the limits of the frequency at the supply voltage. To conduct the scientific experiments we choose the maximum frequency to be limited to f_{sw}=*(40-800)kHz* at a voltage supply U_{dd}=*30V*. The value of this voltage is selected by the restrictive conditions for use of a transistor. The result of the numerical simulation of two expressions (expression 2 and expression 3) to change the working frequency is shown in Fig.5.

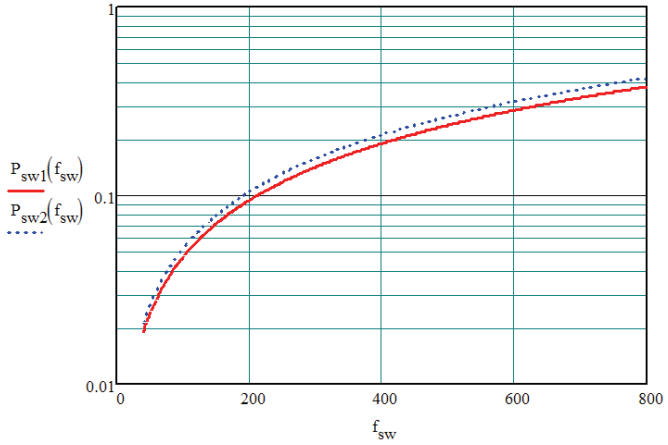

Fig.5. Numerical experiment to define the switching losses P_{sw1} and P_{sw2} with different frequency f_{sw}

From here we can define the following conclusion: While the first numerical experiment is reported in a large discrepancy in the initial values of load current, here inverse relationship is observed. At low frequency both expressions derived approximately the same result. The additional parameters of the study are: C_{oss}=*190pF;* U_{dd}=*30V;* I_d=*1A;* t_r=*10ns;* t_f=*10ns*

Examination also shows that changing the operating frequency significantly affects the growth of the switching losses. To avoid this shortcoming I recommend working frequencies below 400kHz.

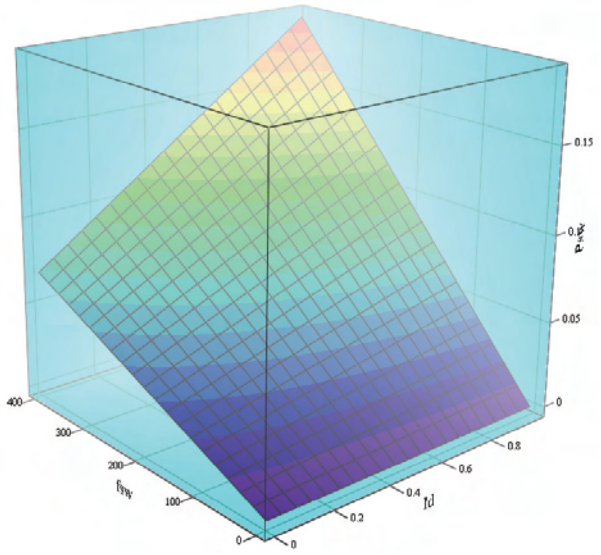

Fig.6. Numerical simulation of the switching losses P_{sw1} with different switching frequency f_{sw} and load current

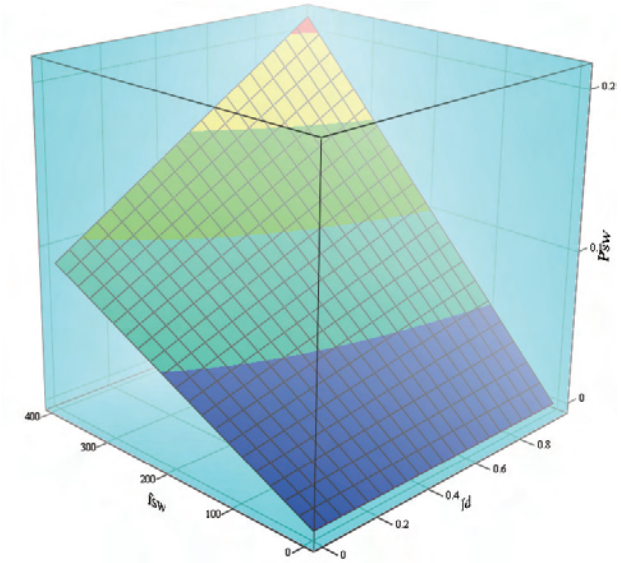

Fig.7. Numerical simulation of the switching losses P_{sw2} with different switching frequency f_{sw} and load current

D. Numerical simulation to identify the switching losses for the simultaneous amendment of the two parameters - Load current and operating frequency

For conducting the research we should comply with the restrictive conditions of a few experiments. This means that the variation in load current will be I_d=*(0,1-1)A*, while the frequency should be amended in the range f_{sw}=*(40-400)kHz*. These results are shown in fig.6. and fig.7 On fig.6 are depicted the switching losses estimated at the first expression, until fig.7 shows the result of expression 2. The result obtained in both studies clearly shows the same variation of switching losses regardless of the chosen method. It is striking low divergence of results in minimum values of output current and maximum operating frequency.

E. Numerical simulation to identify the switching losses by changing the voltage supply

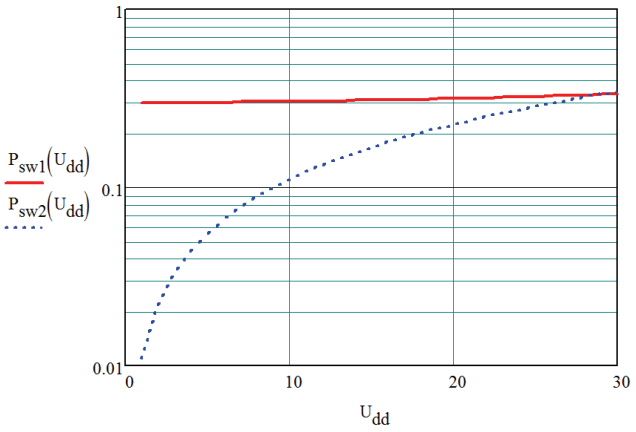

Fig.8. Numerical simulation of the switching losses P_{sw1} and P_{sw2} with parameter the voltage source.

For the purposes of the scientific experiment let us change the voltage supply varying by the value U_{dd}=1-30V. On the other hand the switching frequency is f_{sw}=200kHz. The purpose of the numerical simulation is the comparison of the switching losses P_{sw} on the both familiar mathematical expressions [1], [2].

The programmable result is shown in fig.8. The study shows a significant discrepancy between the results for P_{sw1} and P_{sw2} At low values of this voltage the results for P_{sw2} suggest low switching losses while the value of power around U_{dd}=30V readings are approaching a significant. Additional parameter of the numerical experiment is: C_{oss}=190pF; U_{dd}=30V; I_d=0,1-1A; t_r=t_f=10ns. The conclusion is that within a range of the study values obtained for the switching losses differ significantly. Out of the experiments we observe a point of intersection of characteristics about voltage U_{dd} = 30V, but they are not allowed to be criteria for the assessment.

F. Numerical simulation to identify the switching losses by changing the switching frequency

For the proper implementation of this numerical simulation it is necessary to set limits on the frequency at constant voltage. To conduct scientific experiments the limits of the operating frequency are consistent with practical PCM digital audio systems in the operation range f_{sw}= 40-800kHz In this case the power supply voltage is kept constant U_{dd}=30V.

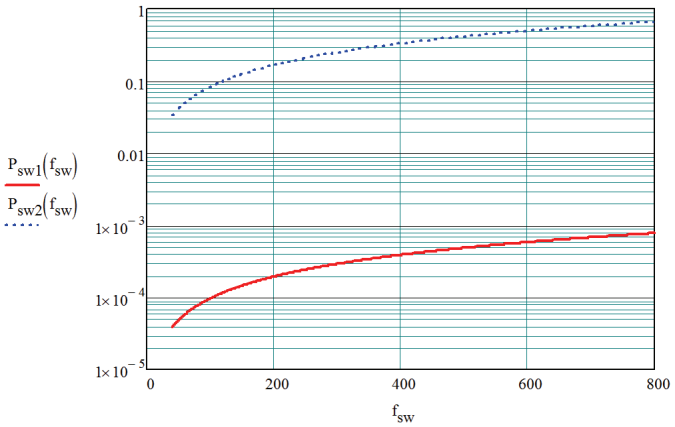

Fig.9. Numerical simulation of the switching losses P_{sw1} and P_{sw2}

The exact value is selected from the data of the first experiment. The result obtained by the numerical simulation of expression 2 and expression 3 with changing the switching frequency is shown in fig.9.

From the result obtained we notice significant discrepancy of the results. From there we can define the following conclusion: The first numerical experiment shows that the reported values for P_{sw2} are lower or equal to P_{sw1}, while the second switching losses P_{sw2} are reported as significantly lower. Additional parameter of the numerical experiment is: C_{oss}=190pF; U_{dd}=30V; I_d=1A; t_r=10ns; t_f=10

IV. Conclusion

- In this numerical simulation it is necessary to determine the limits of the frequency at the supply voltage. In order to conduct the scientific experiments we choose the maximum frequency to be limited to fsw=(40-800)kHz at a voltage supply of Udd=30V;
- While the first numerical experiment is reported in a large discrepancy in the initial values of load current, here we observe inverse relationship. At low frequency both expressions derived approximately the same result.
- There are minimal differences at low currents Id, but they can not be criteria for the assessment of the wall range;
- The outcomes of the research suggest that the results of both methods can be compared over a limited drain current Id> 0,2 A. This current is equal to one fifth of the maximum, which is defined by the moshtnosts output and supply voltage.

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