Experimental Setup for BER Measuring of Free Space Optical System

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Abstract – **The paper describes measuring of BER during data transmission in FSO system. The used transmitting and receiving electronic blocks are connected in suitable manner with the designed by the authors BER testing system. The system is installed on the blocks 1 and 2 of the TU-Sofia. Preliminary results about system availability are presented.**

Keywords– **Bit Error Rate, Free Space Optics, Bit Error Rate Tester.**

I. INTRODUCTION

The bit error ratio (BER) is a measure of the percentage of bits that a system does not transmit or receive correctly. It is a dimensionless number ranging from 0 to 1. If the BER = 0, then all bits are transmitted correctly at the other extreme, if the BER = 1, every bit is received in error. Every transmission system (and every part of it) has an intrinsic bit error ratio, which can take on any real number between 0 and 1. The exact value may change, for example, with temperature or operating voltage, but it's a fundamental system property[1].

$$BER=Nerr/Nall \quad (1)$$

whereNerr - number of mistaken bits, Nall - number of all bits. It's very important constructed FSO system to be tested for BER in real atmospheric conditions [2, 3].

II. SCHEMATIC DESIGN

The device which is measuring the level of error BER is called BERT bit error rate tester. This article describes exactly such a scheme for measuring the BER [4].

Block diagram and real photos of the system is shown in Fig.1.The information is transmitted simultaneously on two channels one is atmospheric and the other is a conductor.

Once the information passing through both channels of their output signals are compared in the block BER measure. If there is a difference in the two signals the counter COUNTER shows an counts on the display. Since the delay of the signal varies in both channels they are connected delay elementsto thescheme. Delays are implemented in two ways.

The random number generator is realized by shift registers and logic elements exclusive OR (XOR) shown in Fig.2.The

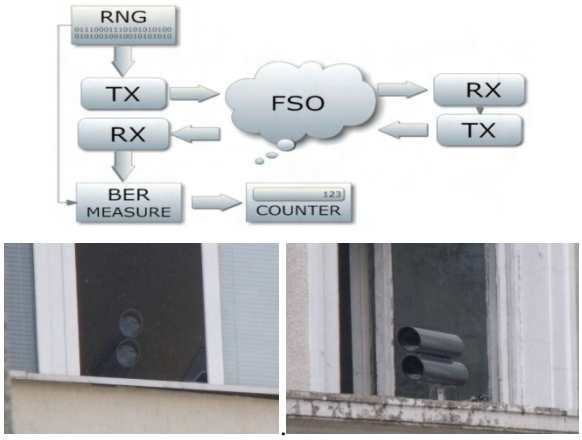

Fig. 1. Block scheme and real pictures of FSO

information is shifted on every tick of the clock generator from left to right, and last but one and last digit are connected to both inputs of the logical element XOR. After completion the logical operation result is returned to the first digit of the

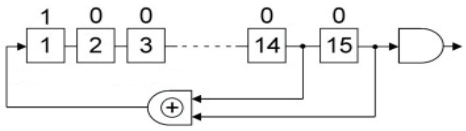

Fig. 2. Scheme of random number generator

shift registry, etc.

Fig.3 shows the principal realization of the random number generator.The shift registers are realized with integrated circuit 74HCT174 and a logic element exclusive OR with 74HC86. The circuit is supplied with voltage 5V. Clock signal is necessary for normal operation of the scheme. It is fed to the ninth pins of integrated circuits 74HC174.

Thecoarse delays of n number of ticks is implemented with D flip flops Fig.4. Depending on the required number of ticks of delay a different number of D flip flops are used [5].For shorter delays are used non-inverting buffers.

For comparison of two signals from the optical path and conductorare used logic element exclusive OR (XOR) Fig.5. To avoid error in the divergence of the two fronts of the signal after XOR logic element is added a logic element AND is added, comparing the two signals only when the clock signal is in high level.

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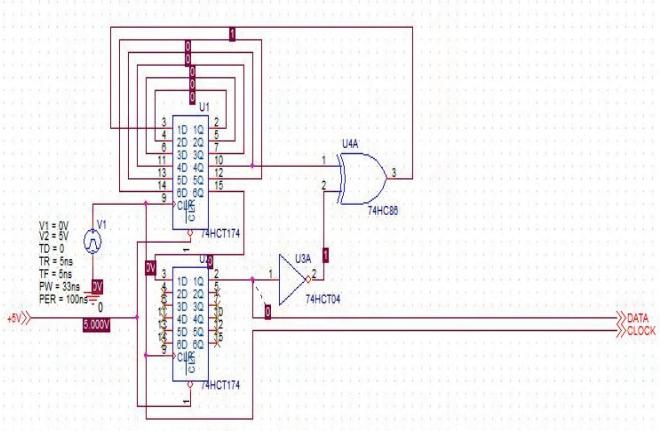

Fig. 3. Principal realization of random number generator

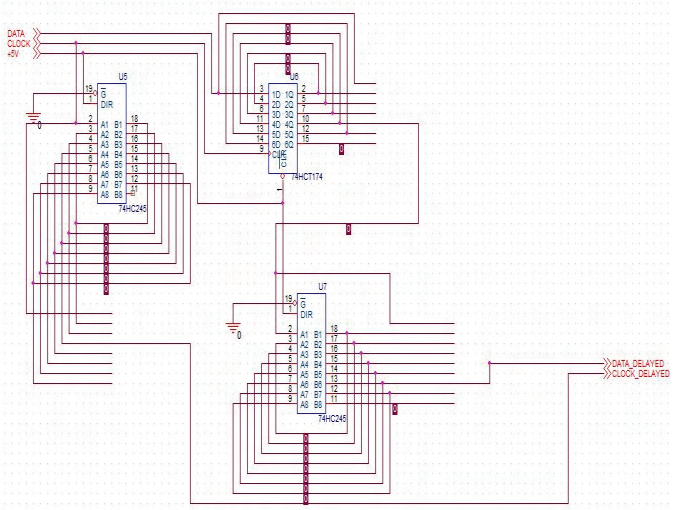

Fig. 4.Principal realization ofscheme for long delays

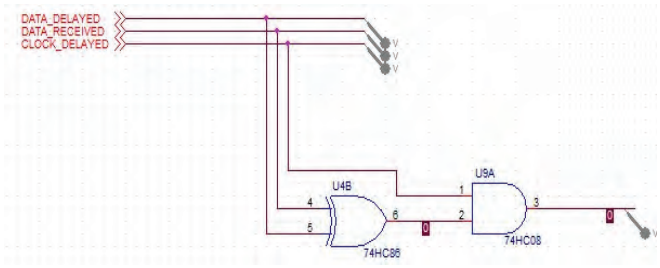

Fig. 5. Principal realization of comparing scheme

III. SIMULATION

Fig.6 and Fig.7 shows two computer simulations. In Fig.6 can be seen an error caused by misalignment of the two edges of the pulses: the first is the transmitted data and the second is the delayed original data. In Fig.7 the signals are aligned in time at which the error does not occur. Error signal at output of the scheme is low level.

The speed of FSO link is 10Mbps. The distance between Rx and Tx is 180 m. The receiver bandwidth is 16MHz. The spot size at the receiver is 900mm. The receiver aperture is 90mm.

We left the system to work for a week, but the whether conditions prevented the accumulation of any error.The

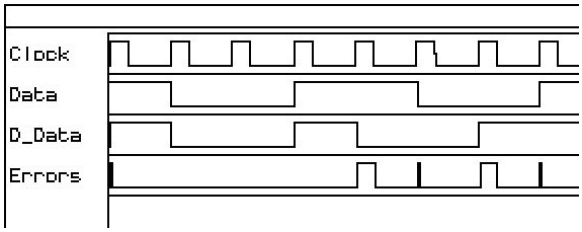

Fig. 6. Computer simulation of errors

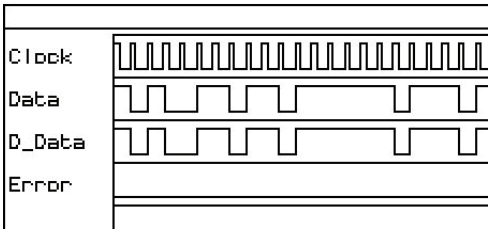

Fig. 7. Computer simulation without errors

nominal working distance of the system is 1km, but in the particular case we worked at 180 m. This also prevents accumulation of error.

IV. CONCLUSION

The described scheme can be appliedfor studding the dependence of the level of bit error of Free Space Optics systems and the dependency of destabilizing factors such as atmospheric conditions (fog, snow, rain, etc.). [6, 7]. In future we plan to work at nominal distance and with bigger time intervals witch will enable accumulation of error.

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