FPAA Implementation of Phase-Independent Synchronous Detector for Spectrum Analyzer

Eltimir Stoimenov[1], Georgi Mihov[2], Ivailo Pandiev[3]

Abstract – **This paper presents a phase independent synchronous detector based on Field Programmable Analog Array (FPAA) devices. The proposed synchronous detector consists of two one-quadrant analog multipliers and two first-order low-pass filters (LPFs). The 'modus operandi' could be explained with the multiplication of the input signal with two additional reference sine and cosine signals with varying frequency. This way the resulting DC offset is proportional to the magnitude of the spectral component with frequency equals the frequency of the referent signal. The circuit is phase independent due to the output block for vector sum. The output voltage corresponds to the half amplitude of the specific spectral component. The functional elements of the structure are realized by employing configurable analog modules (CAMs) of the FPAA AN231E04 from Anadigm. The detector has relatively wide-band frequency response and can operate with 3,3V single supply voltage. The simulation results show good agreement with theoretical analysis.**

Keywords – **Analog signal processing, Spectrum analysis, Synchronous detector, Circuit for modulus calculation, FPAA.**

I. INTRODUCTION

The spectral analysis is quite a common task in nowadays electronics. Almost all devices doing spectral analyses rely on digital signal processing and more specifically - Fast Fourier Transform (FFT) [3]. Although digital signal processing possess many advantages like high noise immunity, high accuracy and great flexibility, depending from the application, this method could possess certain drawbacks. The most obvious of them is the need of sophisticated and relatively expensive microprocessor system. This could lead to increased overall power consumption and greater PCB requirements.

In the current paper we have recourse to a somewhat outdated method for spectrum analysis. It is based on purely analog circuits for signal processing and is already known in the literature [1],[2]. This method is implemented by a specific class of electronic circuits called "Synchronous detectors (or synchronous demodulators)". This kind of circuits is widely used in balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication [4]. The synchronous detectors are circuits which are highly selective and can obtain the amplitude of a spectral component with certain frequency of a noisy signal. The detector is controlled by an external signal with sinusoidal form. A detailed mathematical description of circuit operation is given in a section entitled "Principle of operation".

In addition, we have to note that the circuit described in this paper is planned to work in co-partnership with a specific digital control system introduced in [5]. In that way a Collaborative Analog and Digital Signal Processing (CADSP) system is realized.

II. PRINCIPLE OF OPERATION

The principle of operation of the phase-independent synchronous demodulation is based on multiplication of the input analog signal with sinusoidal and cosinusoidal signals with a certain frequency f_{CS}. The separation of the DC voltage proportional to the amplitude and the phase of the harmonic with frequency f_{CS} is performed by a low pass filter. The output voltage of the phase-independent synchronous detectors is obtained by vector sum circuit. As a result the output DC voltage is proportional only of the amplitude of the input signal with frequency f_{CS}.

The block diagram of the phase-independent synchronous detector implemented in our research is shown on Fig. 1. It's consisted by two one-quadrant analog multipliers, two LPFs and one output block for modulus calculation. The input x of the multipliers is connected to the input signal, while the y input is applied with sinusoidal (sin) and cosinusoidal (cosine) signals u_1 and u_2 from a quadrature generator. These signals are synchronizing and can be described by the fallowing equations:

$$u_1 = E\sin(\omega_{GEN}t) \quad u_2 = E\cos(\omega_{GEN}t) \tag{1}$$

Here E is the amplitude of the signals and ω_{GEN} is its frequency.

We will assume that the input signal u_i is a sine waveform with equation:

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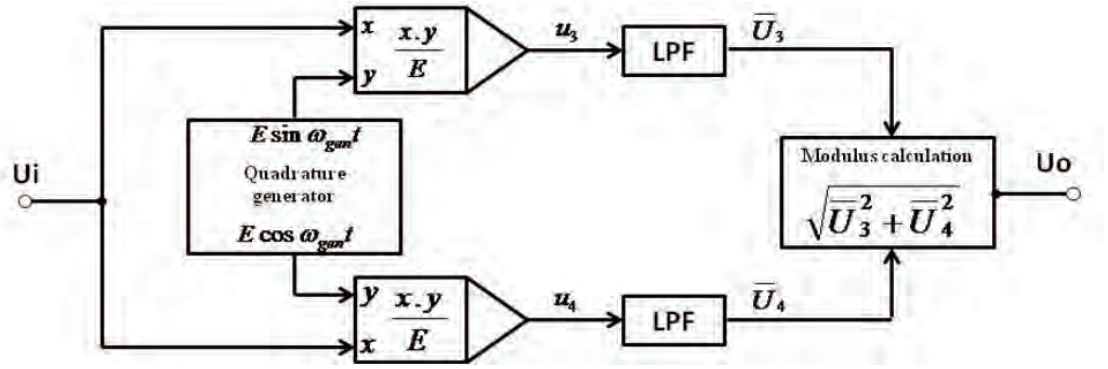


Fig. 1. Phase-independent synchronous detector block diagram.

$$u_i = U_{im}\sin(\omega_{in}t + \varphi) \tag{2}$$

where φ is the phase and u_{im} is the amplitude of the signal.

After multiplication the resulting signals from the analog multipliers can be described as:

$$u_3 = \frac{1}{K}[U_{im}\sin(\omega_{in}t + \varphi).E\sin(\omega_{GEN}t)] \tag{3}$$

$$u_4 = \frac{1}{K}[U_{im}\sin(\omega_{in}t + \varphi).E\cos(\omega_{GEN}t)] \tag{4}$$

where $\frac{1}{K}$ is a multiplication factor. Assuming that $K = E$ and, we can simplify the above equations to:

$$u_3 = U_{im}\sin(\omega_{in}t + \varphi).\sin(\omega_{GEN}t) \tag{5}$$

$$u_4 = U_{im}\sin(\omega_{in}t + \varphi).\cos(\omega_{GEN}t) \tag{6}$$

Using the trigonometric relations:

$$\sin\alpha.\cos\beta = \frac{1}{2}[\cos(\alpha+\beta) - \cos(\alpha-\beta)] \tag{7}$$

$$\sin\alpha.\sin\beta = \frac{1}{2}[\cos(\alpha-\beta) - \cos(\alpha+\beta)] \tag{8}$$

we can further evolve the above equations:

$$U_3 = U_{im}\sin(\omega_{in}t + \varphi).\sin(\omega_{GEN}t) =$$
$$= \frac{1}{2}U_{im}[\cos(\omega_{in}t + \varphi - \omega_{GEN}t) - \cos(\omega_{in}t + \varphi + \omega_{GEN}t)] \tag{9}$$

If we assume that the input frequency is equal to the frequency of signal from the DDS generator, or $\omega_{GEN} = \omega_{in}$ we have:

$$U_3 = \frac{1}{2}U_{im}\cos(\varphi) - \frac{1}{2}U_{im}\cos(2\omega_{GEN}t + \varphi) \tag{10}$$

Similarly for U_4 we get:

$$U_4 = \frac{1}{2}U_{im}\sin(\varphi) - \frac{1}{2}U_{im}\sin(2\omega_{GEN}t + \varphi) \tag{11}$$

If we analyze equation (9) we can infer that output signal from the multiplier is a sum of two sinusoids, one with low frequency and the other with high frequency. But when $\omega_{GEN} = \omega_{in}$ the first term of the signal is a DC and the second one is a sinusoidal component with doubled frequency. When we apply this signal to the input of LPFs with very low corner frequency only the DC component will pass. Consequently the output signals from the LPFs will look like equations (11) and (12).

$$\overline{U_3} = U_{im}\cos(\varphi) \tag{11}$$

$$\overline{U_4} = U_{im}\sin(\varphi) \tag{12}$$

We can generalize:

$$\overline{U_3} = \begin{cases} \frac{1}{2}U_{im}\cos(\varphi), \text{ when } \omega_{GEN} = \omega_{in} \\ 0 \qquad\qquad , \text{when } \omega_{GEN} \neq \omega_{in} \end{cases} \tag{13}$$

$$\overline{U_4} = \begin{cases} \frac{1}{2}U_{im}\sin(\varphi), \text{ when } \omega_{GEN} = \omega_{in} \\ 0 \qquad\qquad , \text{when } \omega_{GEN} \neq \omega_{in} \end{cases} \tag{14}$$

As it's obvious U_3 and U_4 are proportional to the amplitude U_{im} and the phase φ of the input signal.

The last block in the system performs modulus calculation of $\overline{U_3}$ and $\overline{U_4}$. Its output signal $\overline{U_O}$ is:

$$\overline{U_0} = \frac{1}{2}U_{im}\sqrt{\sin^2(\varphi) + \cos^2(\varphi)} = \frac{1}{2}U_{im} \tag{15}$$

As we can see, thanks to that block the output signal is only proportional to U_{im} and is phase independent to the input phase φ.

III. System Realization

The realization of the system described above could be quite challenging as it contains relatively complex and hard to attune analog blocks. Fortunately, recently the market introduced somewhat new class of devices called Field Programmable Analog Arrays (FPAA). These devices allow easy implementation of rather complex analog transfer functions. This could reduce the development time significantly and consequently, made FPAA our choice for realization.

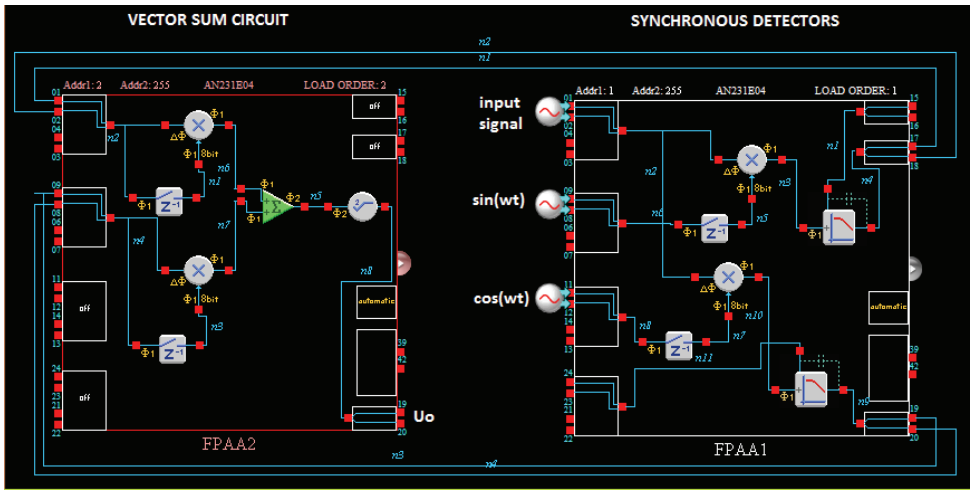


Fig. 2. FPAA configuration of synchronous detector from Fig. 1.

Any FPAA device is consisted by specific number of the so called Configurable Analog Blocks (CAB). These blocks implement Switching Capacitance (SC) technology and could be configure very flexibly. The CABs are surrounded by programmable interconnect resources for signal tracing from one CAB to other. Also FPAA incorporates analog input / output cells which can be set up in variety of operating modes. Using the software development environment the user can built the desired circuit with ease using numerous of predefined analog blocks. These blocks include amplifiers, sumators, integrators and many more.

The main drawbacks of FPAA technology are the reduced bandwidth and the increased power consumption compared to their application specific counterparts. Nevertheless we have to note that these disadvantages are not important to our system, as it haven't been planned to work with high frequency or autonomous supply. More detailed information about FPAA could be found in [6],[7].

As to the authors knowledge there is only one FPAA manufacturer on the market - Anadigm Inc. The company offers a wide range of silicon devices and software development tools. We have decided to use AN231K04-DVLP3 AnadigmApex Development Board as a hardware platform.

For realization of the system we've used Anadigm Designer 2 IDE. The screenshot shown on Fig. 2 presents our concept. The system is built with two FPAAs so two development boards should be daisy chained. Despite that intuitively the signal flow should be from the left Integrated Circuit (IC) to the right, the ICs are placed reversed (the input signals are applied to the right IC). The reason for this is technical and is due to the fact that the development boards could be daisy chained only from right to left (reverse to the signal flow). The right IC consist the two synchronous detectors and solves Eq. (2), (3) and (4). As the LPF should pass only the DC component, the corner frequency of the filter should be as low as possible. Therefore we used LPF with external capacitor which can achieve corner frequency as low as 10-2 Hz. The FPAA input analog signals are referenced to $VMR = +1{,}5V$ (Voltage Mid-Rail − VMR) and are limited to the range of 0 to $+3{,}3V$.

As already mentioned the multiplication factor K should be equal to the reciprocal of the amplitude E of the sine and cosine signals. So if we use signals with amplitude $E = 1{,}25V$ we can determine that $K = 0{,}8V^{-1}$.

The circuit implemented in the left FPAA performs the modulus calculation and solves Eq. (5). It is consisted by two multipliers operating as squarers, summator and square root extracting circuit.

The maximum operating frequency (corner frequency) of the detector is approximately 50 kHz.

IV. Simulation Results

The workability of the proposed synchronous detector shown on Fig. 2 is presented through simulation results. All the simulations were conducted using AnadigmDesigner2 IDE.

All the three simulations aim to show the ability of the system to obtain the spectrum of different kind of input signals. The simulation set up parameters are as follows: amplitude of the input signal (U_{im}) - 0,8 V; amplitude of the quadrature generator signals (E) - 1,25 V; multiplier multiplication factor (K) – 0,8 V^{-1}; all input signals DC offset - 1,5 V; Simulation time – 5ms.

We have to note that for simulation purposes the quadrature generator is replaced with two sinusoidal generators. The first of them forms the sine signal, while the other is set up with 90° phase shift so a cosinusoidal signal can be formed.

The simulation procedure is as follows: firstly an input signal with desired parameters is applied to the system. Then the frequency of the quadrature generator is incremented with some step and the respective output voltage is recorded. The iteration is repeated till the desired frequency band is achieved.

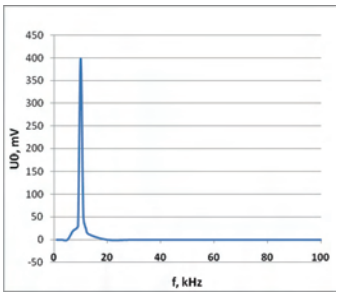
The simulation results are shown in Fig. 3. In the first case, shown on Fig. 3a, the input signal is a pure sinewave. Theoretically the spectrum of such a signal should look like a sharp spike. The maximum of this spike must be reached when x-axis become equivalent to the frequency of the input

signal. Also its amplitude should be $\frac{1}{2}U_{im}$ (400 mV in the current case).

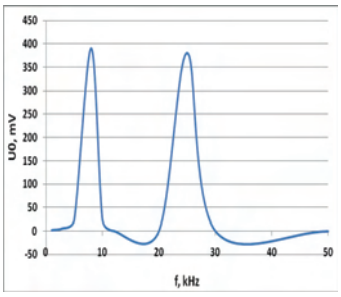
The second study is conducted with an input signal constituted by two sinewaves. The one sinewave is with frequency $\omega_{1in} = 8kHz$ and the other is $\omega_{2in} = 25kHz$. The amplitude should be still about 400 mV (Fig. 3b).

The third case, shown on Fig. 3c, examines squarewave input signal with frequency $\omega_{in} = 10kHz$. As it is well known from the theory the spectrum of such a signal is the *sinc* function with extremums multiple of the input frequency.

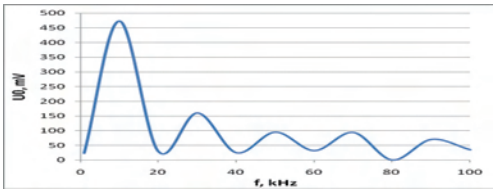
The last study is conducted with Electrocardiographic Signal (ECG) shown on fig. 3d. The analyzed signal is shown on fig. 3f. The spectrogram shown on fig. 3e is given with comparison purposes and it's obtained with specialized software "FFT Properties v5 trial" from Dew Research Inc[8]. Unfortunately there is poor agreement between the two spectrograms. Nevertheless we have to note that the spectrogram is quite complex and probably more simulation points will improve the situation (currently the spectrogram is built with 20 points). Also we have to mention that for simulation purposes the frequency of the ECG signal was increased 1000 times. The reason for this frequency increasing is that under simulation Anadigm Designer 2 doesn't allow the usage of LPF with external capacitors. As already mentioned, for simulation purposes we have been forced to use an ordinary LPF which have pretty higher corner frequency.



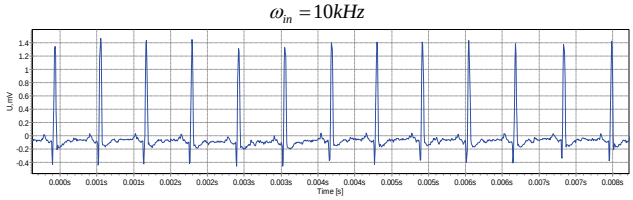
a) Pure sinewave with frequency $\omega_{in} = 10kHz$



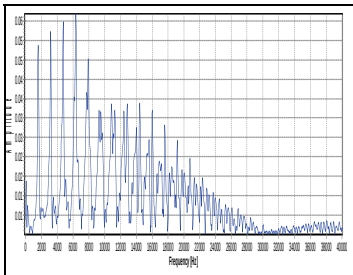
b) Sum of two sinewaves with frequencies $\omega_{1in} = 8kHz$ and $\omega_{2in} = 25kHz$



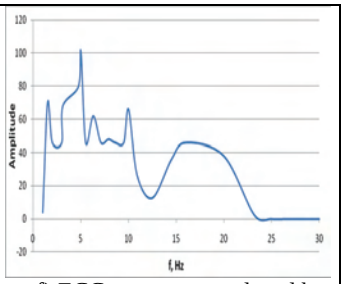
c) Square wave signal with frequency $\omega_{in} = 10kHz$



d) ECG Input Signal



e) ECG spectrum produced with FFT properties trial [8]



f) ECG spectrum produced by SD simulated with Anadigm Designer 2

Fig. 3. Simulation results with different input periodic signals.

V. Conclusion

In this paper a SD independent to the signal phase has been proposed. The SD circuit consists two one-quadrant analog multipliers, two first-order low-pass filters with external capacitors and output block for modulus calculation. The circuit is synchronized by two control signals with sine and cosine form. If the frequency of these signals varies linearly the SD could be used as a spectrum analyzer. A detailed mathematical description of the circuit operation was given. Also for confirmation of the theoretical predictions various simulations has been conducted.

Acknowledgement

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