Design of Digital Control System of Spectrum Analyzer Built on MicroBlaze™ Processor

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Abstract –**The modern spectrum analyzers rely on purely digital signal processing methods such as Fast Fourier Transform (FFT). In some application multiresolution methods such as Wavelet are also applied. Regardless of the specific implementation the methods discussed above relies on digital system data processing. We are proposing a different approach for obtaining the spectrum of an input signal which relies on Collaborative Analog and Digital Signal Processing (CADSP). The current paper presents the design phase of a digital control system for a spectrum analyzer exploiting CADSP. The system is planned to be realized with Spartan3E Starter Kit equipped with onboard Field Programmable Gate Array (FPGA). It includes quadrature Direct Digital Synthesis (DDS) generating block, control unit, memory and some minor logical blocks ,all of them implemented in the FPGA. The control unit is based on Microblaze software processor with some additional periphery and it is in charge of managing all the system operations. These operations include - transferring the data from the DDS block to the onboard digital-to-analog converter (DAC) and servicing the user interface. The analog circuitry of the spectrum analyzer is realized with Field Programmable Analog Array (FPAA) and it is discussed in details in [1]. The proposed controlling system for spectrum analyzer is in a process of realization and experimental testing.**

Keywords – **Spectrum analysis, DDS function generators, Microblaze, CADSP, FPGA.**

I. Introduction

Spectrum analysis of an input signal is a common task in various fields of electronics. The modern approaches rely almost fully on digital signal processing and FFT in particular. This paper and [1] presents a different approach for spectrum analyzing based on mixed (analog and digital) signal processing. Using such an approach could poses some advantages like reduced power consumption, reduced size on chip and even higher computing performance, compared to its purely digital counterparts. In the heart of the spectrum analyzer mentioned above is the so called Synchronous Detector (SD). This purely analog circuit performs all the complex computing operations. Thanks to that circuit the harmonic composition of the input signal could be obtained. Detailed information about this kind of circuits could be found in[1], [2] and [3]. Nevertheless we should note that for proper operation of the analyzer the SD needs some additional circuitry. This includes circuitry for data collection and, more important, specific quadrature generator. The generator should be able to produce sine and cosine signals with varying frequency and. Also they should be with high signal to noise ratio (SNR) and swing not exceeding 3,3 V. The easiest way for generating such signals is the usage of DDS which can satisfy all these requrements. Detailed information about DDS can be found in [4].

This paper introduces a design of the system that will provide all the necessary functionalities needed by the SD for proper operation.

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II. Block Diagram

The first stage in designing the system described above is the synthesis of the block diagram. The blocks needed for realization are: quadrature DDS generating block, controlling block (processor) and user interface.

A. Processor block

The processor block is responsible for the entire control tasks in the system. The processor should have sufficient memory and peripheral recourses. Its performance isn't critical as all the complex signal processing tasks are carried out in the analog part as described in section I.

B. Quadrature DDS generator block

The output signals from the DDS block are vital for proper operation of the SD. The required signal parameters are: simultaneous sine and cosine outputs, varying frequency up to several kHz, pick to pick swing limited to 0 - 3,3 V, signal to noise ratio (SNR) and frequency tuning resolution should be as high as possible.

C. User interface

The user interface should contain standard devices like LCD, push-buttons and RS232 interface. This block allows the user to communicate with the system and set all the parameters of interest.

D. Interface to the SD

As our system relies on the collaboration between analog and digital signal processing the problem for proper data exchange between the two parts arises. The natural solution of this problem is the usage of DAC and ADC. The DAC should convert the signals from the DDS block in appropriate analog form. On the other hand the ADC allows data receiving from the analog segment of the system.

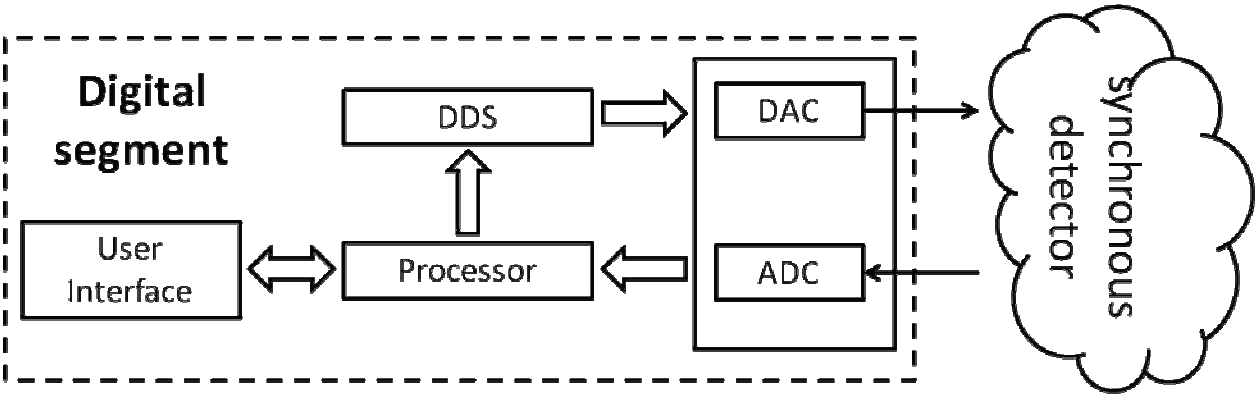

Fig. 1. Spectrum analyzer digital segment block diagram.

III. CONTROL SYSTEM IMPLEMENTATION

For implementation we've decided to use Spartan-3e Starter Kit from Xilinx Inc. This kit is very well known among the electronics engineering community and a plenty of information about it is available in internet. Moreover it possesses all the necessary blocks onboard. The kit is equipped with Spartan3E FPGA which will be extensively used in the system implementation. For more detailed information about the kit you can address to [7].

For software design environments Xilinx ISE and Xilinx EDK tools will be used.

If we refer to fig. 1 we can note that all the blocks, except ADC and DAC, could be implemented in the onboard FPGA. A block diagram with the components implemented in the FPGA is given on fig. 2. Also a detailed description will be given below.

Also now is the right moment to note that the starter kit has onboard devices like LCD, LEDs, pushbuttons and rotary encoder which are very convenient for user interface realization.

A. GPIO and Rotary switch encoder blocks

These blocks are part for the user interface which serves as a connection to the user. The GPIO block connects the system to the onboard pushbuttons, LCD and LED indicator. The Rotary switch encoder block filters the glitches from the externally connected rotary switch and that way unloads the processor from this task.

B. DDS Generating block

This block has a major role in the system and must provide the appropriate signals, needed by the SD circuit. The block is synthesized using Xilinx ISE prewritten IP core. The following key parameters were set:

- Type of output signals : Sine and Cosine
- Frequency tuning resolution : < 2Hz
- Output data width : 14 bits

C. Processor block

For system control our development exploits MicroBlaze software processor. The MicroBlaze core is a 32-bit RISC Harvard architecture soft processor with a rich instruction set optimized for embedded applications. The MicroBlaze processor, allows complete flexibility to select the combination of peripheral, memory and interface features that will give the exact system needed [5]. According our needs we've synthesized the processor putting up the following blocks and parameters:

- 32kB of Data and Instruction memory. Of course, Local Memory Buses and Memory Controllers are included.
- GPIOs – for connection with external or internal modules like LEDs, LCD and DDS block.
- Timers – for generating different time intervals
- Interrupt system - for servicing the interrupts from GPIOs and timers
- SPI for communication with DAC and ADC circuitry
- UART interface for PC connection
- Processor System Reset and Clock Generator.

The program algorithm of the processor is described in section IV.

D. ADC and DAC block

The Spartan-3E Starter Kit board includes ADC and DAC circuitry which are very convenient for connection with the analog circuitry. The DAC device is a Linear Technology LTC2624 quad DAC with 12-bit unsigned resolution. It is SPI-compatible, four-channel, serial Digital-to-Analog Converter. Two of the channels of the DAC are referenced to 3,3 V and the other twos to 2,5 V. We will use the 2,5 V referenced channels for sine and cosine production.

For analog signal input we are using the onboard analog capturing circuit. The circuit consists of a Linear Technology LTC6912-1 programmable preamplifier that scales the incoming analog signal. The output of the pre-amplifier connects to a Linear Technology LTC1407A-1 ADC. The reference voltage for the amplifier and the ADC is 1,65V. The

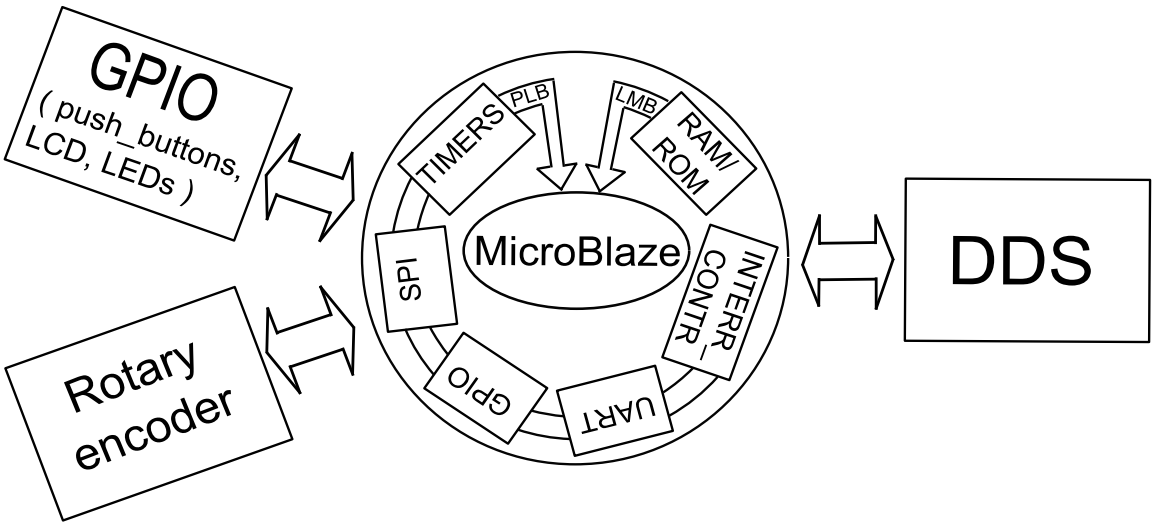

Fig. 2. FPGA – Block structure.

ADC presents the digital representation of the sampled analog values as a 14-bit, two's complement binary value [6], [7]. Both the pre-amplifier and the ADC are serially programmed or controlled by the FPGA [7].

IV. MICROBLAZE PROGRAM ALGORITHM

As already mentioned, the complex signal processing is performed by the analog part of the system so the processor program algorithm is quite simple. First of all the processor should control the output frequency of the DDS block in such a way that a linear sweep is formed. This is achieved in the main loop by incrementing the Frequency Tuning Word (FTW) on regular intervals Δt with some STEP value. When FTW reach the MAX value the process repeats. The user should take care for appropriate set of MAX, MIN, Δt and STEP constants through the user interface (push-buttons, rotary encoder and LCD).

Another important task of the processor is to transmit the output data from the DDS block to the DAC through the SPI interface. The program algorithm is shown on the Fig. 3.

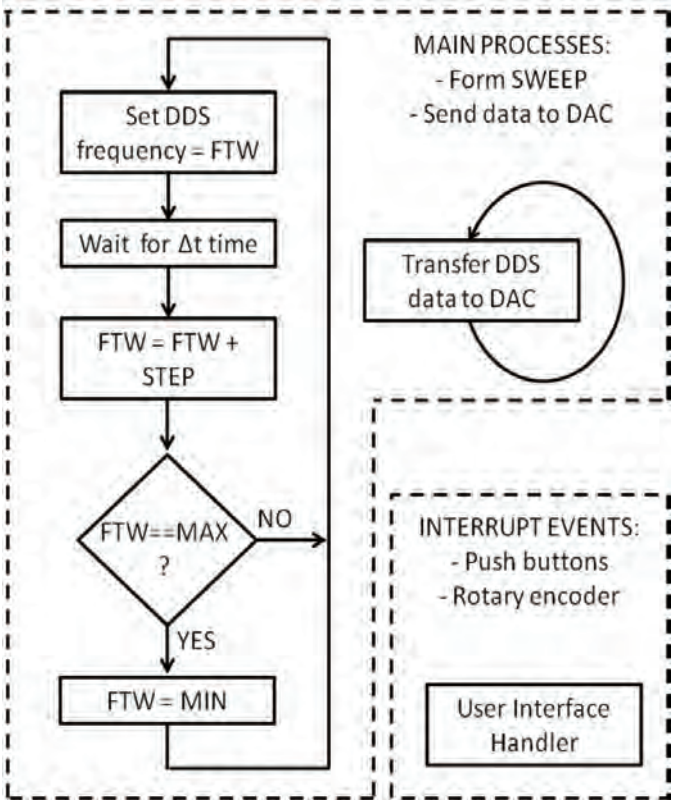

Fig. 3. Microblaze program algorithm.

V. Conclusion

CADSP is very interesting and relatively new engineering solution for signal processing. It exploits the computing power of digital as well as analog circuits which can greatly benefit the system parameters. The current paper presented the design of the digital control system which is a part of a Spectrum analyzer based on CADSP. The design is built around Microblaze soft processor which is charge for all the system control tasks. Moreover a DDS generator was implemented in the FPGA so a specific sine and cosine signals, necessary by the SD, could be produced. The author hopes that system will be realized soon and some experimental results could be reported.

Acknowledgement

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