Body Bias Influence on Ring Oscillator Performance for IR-UWB Pulse Generator in 0.18μm CMOS technology

Jelena Radic, Alena Djugova, Laszlo Nagy and Mirjana Videnovic-Misic

Abstract – **A CMOS standard three-stage ring oscillator is examined in UMC 0.18μm technology. The ring oscillator performance dependence on the bulk (substrate) resistors introduced into inverter PMOS and NMOS transistors is investigated. Simulation results showed that the ring oscillator frequency is strongly dependent on the substrate resistor value. This fact can be used to increase the ring oscillator frequency. As the ring oscillator is a part of an IR-UWB (Impulse Radio Ultra Wide Band) pulse generator, its oscillating frequency determines the central frequency of the pulse spectrum and have significant effect on spectrum fitting within UWB FCC mask.**

Keywords – **Body biasing, bulk resistor, CMOS process, impulse radio ultra-wideband (IR-UWB), ring oscillator.**

I. INTRODUCTION

Impulse Radio Ultra-Wide-Band (IR-UWB) technology has emerged as a potential solution for very high data rate short-range communication, and low data rate communication related to localization, targeting both low cost and low power consumption [1] − [3]. It transmits extremely short pulses, on the order of a nanosecond or less, which occupy a bandwidth up to several GHz. Additionally, IR-UWB technology offers high fading margin for communication systems in multipath environments [3].

The American Federal Communications Commission (FCC) defines a signal as ultra-wideband if it occupies more than 500 MHz of radio frequency spectrum or exhibits a fractional bandwidth of at least 25% [4]. As the FCC allocated frequency spectrum for UWB technology is 3.1 − 10.6 GHz, the power level from the UWB transmitter should be small enough not to interfere with the already existing communication systems such as WiMax, Bluetooth and GSM. This requirement limits output power level of UWB TXs at −41.3 dBm/MHz [4]. In the GPS band (0.96 – 1.61 GHz), there is even more stringent regulation: less than −75.3 dBm/MHz is needed to avoid interference problems. The PSD (Power Spectral Density) in frequency interval from 1.61 GHz to 3.1 GHz depends on the type of application (indoor, outdoor, GPS, wall & medical imaging, through-wall imaging & surveillance system). In spite of these regulations, there have been many reports of interferences with wireless local area network (WLAN) systems operating in the 5 – 6 GHz band. Due to practical reasons, the UWB bandwidth is subdivided into two bands: 3 − 5 GHz (lower-band) and 6 − 10.6 GHz (higher-band).

One of the most critical components of an UWB system is the pulse generator, which has to be designed with relatively low-complexity and low power consumption. Moreover, generated pulse train spectrum has to satisfy the FCC spectral mask, making pulse generator design very challenging. There are several typical techniques for designing it which usually follow all-digital [5] − [6], analogue-digital [7] or all-analogue [7] − [8] design approach. Digital solutions offer higher integration, lower consumption and better controllability while all-analogue techniques demonstrate circuit simplicity.

As an essential part of an analogue-digital pulse generator [5], a ring oscillator is studied in this work. To increase ring oscillating frequency, resistors are introduced between the bulk (substrate) transistors terminals and appropriate voltage terminal (ground in case of NMOS transistor and V_{dd} in case of PMOS transistors). Dependence of the ring oscillator frequency on the value of the bulk resistors inserted in the NMOS, PMOS, and both kind of transistors is examined. The ring oscillator is designed and simulated in 0.18μm CMOS technology.

II. STANDARD THREE-STAGE RING OSCILLATOR DESIGN

The pulse generator represents a key block in the impulse UWB communication. As the pulse shape determines the spectrum characteristic of the UWB signal and effectively dictates specific system requirements, its generation is one of the essential considerations in the UWB design. Fig. 1 shows the basic topology of an IR-UWB transmitter based on ring oscillator as a part of the pulse generator.

It consists of a glitch generator, a switched ring oscillator, a buffer stage and a pulse shaping (band-pass) filter [7]. The glitch generator turns the ring oscillator on/off approximately

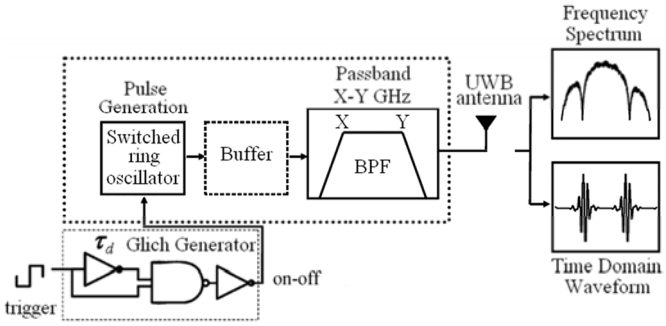

Fig. 1. An IR-UWB transmitter based on ring oscillator as a part of pulse generator.

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defining the duration of its oscillation and thus the width of the pulse generated at the oscillator output. The switched ring oscillator frequency defines position of the transmitted pulse spectrum within the FCC mask [8]. Since in the IR-UWB communication the time domain pulse width roughly determines the width of the generated frequency spectrum [8], it is important to design a pulse, which makes optimal usage of the available spectrum, within the limits imposed by the FCC. The buffer isolates the ring oscillator from the pulse shaping filter loading and improves the pulse generator current driving capability. The band-pass filter additionally accommodates the pulse in the allowed FCC spectral mask.

The switched ring oscillator topology is shown in Fig. 2. It is composed of the three-stage ring oscillator ($M_1 - M_3$ inverters stages) and a pair of oscillation-enabling switches (transistors M_4 and M_5). Due to its simplicity and short start-up time, the ring oscillator is the most used architecture in the IR-UWB transmitter applications. It has small resistance at each feedback nod which allows fast transient response.

The oscillation-enabling switches, as their name says, control the oscillation process. When the *on-off* signal (produced by the glitch generator) is high, M_4 is turned on (M_5 is turned off), the inverters stages $M_1 - M_3$ outputs have initial voltage values determined by the size ratio of the corresponding PMOS and NMOS transistors. Due to the small inverter reactance, the oscillation can start immediately. Transistor M_5 is turned on (M_4 is turned off) at the *on-off* signal low level, connecting the M_1 stage output (the M_2 stage input) to V_{dd}, and effectively shutting down the oscillations. As the ring oscillator is switched off by M_4 transistor during the inactive period of time, the power consumption is minimized.

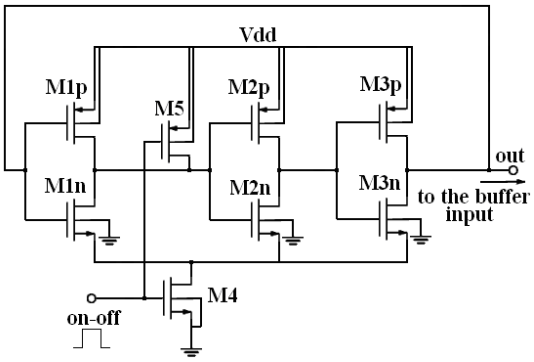

Fig. 2. The three-stage ring oscillator design.

III. THE RING OSCILLATOR PERFORMANCE

The proposed designs have been simulated in mixed mode/RF 0.18µm CMOS technology using SpectreRF Simulator from Cadence Design System. Supply voltage V_{dd} of this technology is 1.8 V. The main problem with the standard ring oscillator design was limited set of transistor sizes available in the used technology as the ring oscillator working frequency depends directly on transistors sizes. If the transistors are larger, the period of the oscillation T rises proportionally, while the oscillating frequency decreases ($f_0=1/T$), and vice versa. For the smallest NMOS and PMOS transistors (transistor width/length: W/L=25µm/0.18µm), the oscillation frequency of 3.95 GHz has been obtained. To utilize the whole UWB band more effectively, the center frequency of at least 6 GHz is required. Higher ring oscillator frequency could be achieved without PMOS transistor M_5. However, this transistor provides the identical oscillation start from the initial state, defined by connecting A' (B) node to V_{dd} at the falling edge of the *on-off* signal.

A. Influence of the NMOS and the PMOS transistors bulk resistors

The bulk (substrate) terminals of the transistors are floated to improve the performance of CMOS SPST (single pole single throw) and SPDT (single pole double throw) switches, especially the power-handling ability and insertion loss, in [9] − [10], respectively. The series transistor particularly played an important role in the switch's insertion loss, while the shunt transistors enhanced the isolation when the switch was turned off. To improve the ring oscillator performance, the method that uses the resistors placed in the inverter stages transistors bulk terminals is investigated in the paper. First, the bulk resistors connected to ground are inserted in the ring oscillator inverter NMOS transistors, shown in Fig. 3.

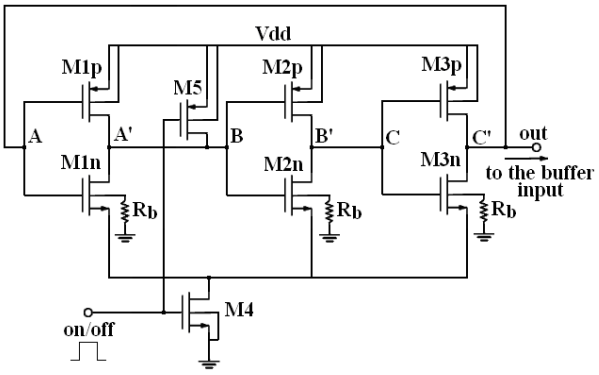

Fig. 3. The ring oscillator with NMOS bulk resistors architecture.

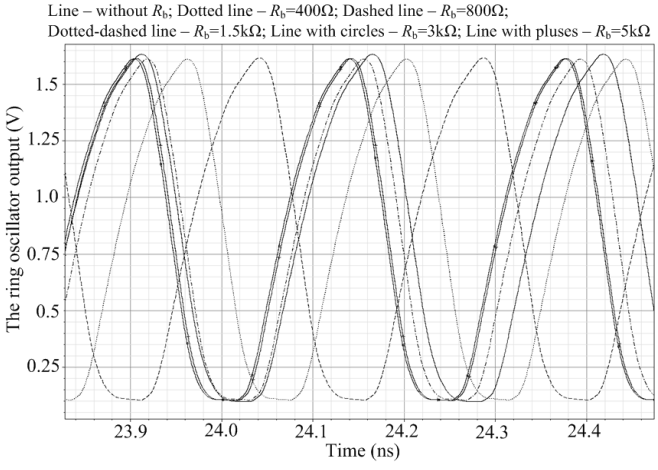

Fig. 4. Dependence of the ring oscillator performance on NMOS transistors substrate resistors values.

Dependence of the ring oscillator performance on the NMOS transistor bulk resistors R_b value is depicted in Fig. 4. It can be noticed that with resistor R_b value increase, the ring oscillator frequency f_0 rises, while the peak-to-peak amplitude at the ring oscillator output changes negligibly. This can be explained by the two effects. First cause, describing the changes in the NMOS transistor threshold voltage V_{tN} by change in the bulk-to-source voltage V_{BS}, is of less concern. This phenomenon is sometimes called the "back-gate effect", since the body influences the threshold voltage when it is not tied to the source, being considered as the second or the "back-gate". The NMOS body effect upon threshold voltage V_{tN} is given by [11]

$$V_{tN} = V_{t0} + \gamma\left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}\right), \quad (1)$$

where V_{t0} is threshold voltage for zero V_{BS} voltage, Φ_F is the Fermi level deep in the bulk, $\gamma = (t_{ox}/\varepsilon_{ox})\sqrt{2q\varepsilon_{si}N_A}$ is the body effect parameter, t_{ox} is oxide thickness, ε_{ox} is oxide permittivity, ε_{si} is silicon permittivity, N_A is a doping concentration, and q is the charge of an electron. With increase in the NMOS transistor bulk resistors value, due to the small substrate current the NMOS bulk voltage becomes slightly positive with respect to the source (the NMOS body-source junction is forward biased), resulting in a low V_{tN} voltage drop. This leads to increase in the current discharging the ring oscillator output and internal node capacitances. As a result, the period of reaching the peak values is decreased and the ring oscillator frequency is increased. Dominant effect represents reduction in the bulk parasitic capacitance current caused by increase in the substrate resistors value. With decrease in the bulk parasitic currents, more current is available for the inverter output capacitance discharging and thus the f_0 parameter rises.

In the second case, the resistors tied to V_{dd} are introduced as the PMOS transistor substrate resistors, Fig. 5. Since the influence on the ring oscillator performance was nearly the same as presented in the simulation above (increase in the PMOS bulk resistors reduces the PMOS threshold voltage V_{tP} and/or decreases the substrate parasitic capacitance currents leading to increase in the current charging the ring oscillator output and internal node capacitances), the output voltage waveform are not given here. However, simulated f_0 values for both approaches are summarized in Tables I, and presented in Fig. 6. Varying R_b from 0.4 kΩ to 5 kΩ, the

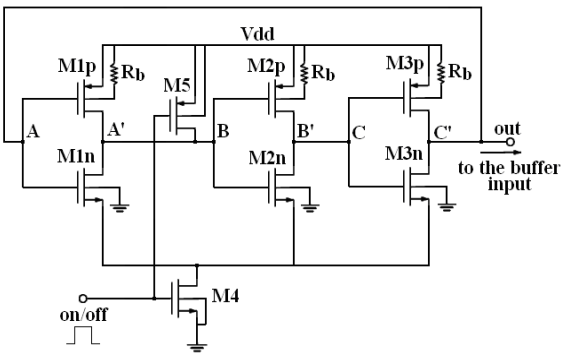

Fig. 5. The ring oscillator with PMOS bulk resistors architecture.

TABLE I
INFLUENCE OF THE NMOS/PMOS TRANSITORS BULK RESISTORS VALUE ON THE RING OSCILLATOR FREQUENCY

	Bulk resistors in NMOS transistors	**Bulk resistors in PMOS transistors**
R_b (kΩ)	f_0 (GHz)	f_0 (GHz)
0.4	4.10	4.0
0.8	4.15	4.10
1.5	4.20	4.20
3.0	4.25	4.25
5.0	4.25	4.25

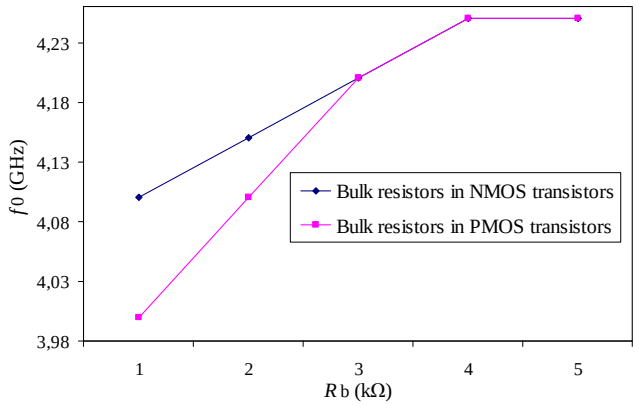

Fig. 6. Dependence of the ring oscillator frequency on the NMOS and PMOS transistors substrate resistors value.

oscillating frequency was increased from 4.1 GHz to 4.25 GHz in case of the NMOS substrate resistors, while f_0 parameter was in the range from 4 GHz to 4.25 GHz for the PMOS bulk resistors method. It can be noticed that for lower substrate resistor values, the higher oscillation frequency was obtained in the former technique. Furthermore, the $f_0 - R_b$ curves go into saturation for the bulk resistor values higher than 3 kΩ in both cases.

B. Influence of the substrate resistors placed in each ring oscillator inverter stage transistor

To further increase the ring oscillator frequency the bulk resistors are introduced in each inverter transistor, shown in Fig. 7. Influence of the R_b value on the ring oscillator

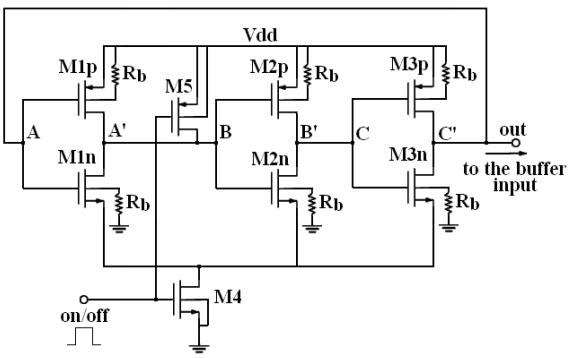

Fig. 7. The ring oscillator with bulk resistor in all inverter's transistors topology.

TABLE II
INFLUENCE OF THE TRANSITORS BULK RESISTORS VALUE ON THE RING OSCILLATOR FREQUENCY

R_b (kΩ)	f_0 (GHz)
0.1	4.0
0.2	4.05
0.4	4.15
0.8	4.35
1.5	4.50
3.0	4.55
5.0	4.60

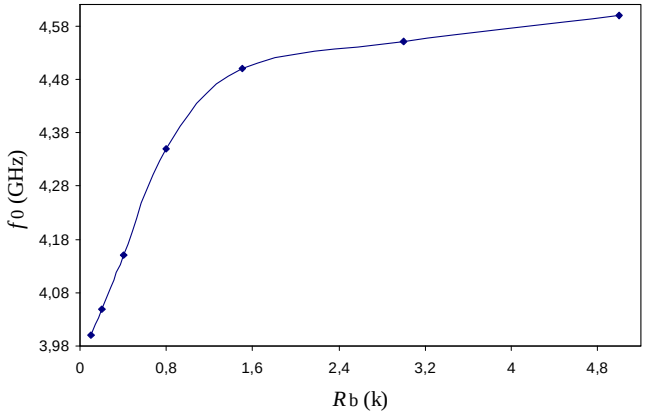

Fig. 8. Dependence of the ring oscillator frequency on the substrate resistors value.

frequency is presented in Table II, and shown in Fig. 8. The same f_0 parameter dependence on the bulk resistor as in the previous simulations can be observed. Nevertheless, it should be emphasized that the achieved ring oscillator frequency is considerably higher comparing to the initial f_o value (3.95 GHz, obtained in the topology presented in Fig. 2), and the values achieved in previous approaches for the same R_b values, as expected.

IV. CONCLUSION

Standard three-stage ring oscillator topology has been analyzed in 0.18μm CMOS technology. Dependence of the ring oscillator performance on the bulk resistors inserted in the inverter NMOS, PMOS, and both kind of transistors has been investigated. Simulations confirmed strong dependency of the ring oscillator frequency f_0 on the substrate resistor value. The maximum frequency (4.6 GHz) obtained in case the bulk resistors were introduced into each inverter stage transistors is remarkably (16.5 %) higher than value achieved with the standard ring oscillator architecture. The f_0 parameter [12] changes can be attributed to the two facts: the NMOS/PMOS transistor threshold voltage drop due to minor increase in the bulk voltage, and/or the parasitic currents reduction, with increase in the bulk resistor value. Both effects cause increase in currents available to charge/discharge the load capacitance and thus the ring oscillator frequency. However, the latter effect is much more dominant.

ACKNOWLEDGEMENT

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