Monolithic Integrated Antennas with High Radiation Efficiency

Hristomir Yordanov[1]

Abstract— **The wireless chip-to-chip interface is an interesting alternative to wired digital buses. An important element from a wireless interconnect is the monolithic integrated antenna. On-chip antennas have to meet several restrictions—they have to cover very little chip area and they need to have high radiation efficiency in a large enough frequency range to allow for fast inter-chip communication. This work describes two methods for designing efficient on-chip antennas, namely using high-impedance substrate with standard thickness, or using very thin substrate.**

Keywords— **Embedded antennas, Near-field communication, On-chip integrated systems.**

I. Introduction

The wired inter-chip interconnects within a system are becoming a substantial bottle-neck for the chip-to-chip digital communications. The wired bus suffers frequency bandwidth limitations due to auto-interference effects like cross-talk and dispersion [1]. These effects can not be reduced by optimising the design of the printed circuit board, because the limitations of that technology have long been met. The standard approach for optimising inter-chip communication is based on using parallel lines and using software techniques like data buffering. The cost of these solutions is increased circuit board complexity. Parallel lines connecting multiple devices result in complicated board layout with very long design time—it is possible to have a multi-layer board design time up to several months.

An interesting alternative to wired chip-to-chip interface is the wireless communication. An efficient wireless interconnect has the potential to offer data rate higher than its wired counterpart, while keeping the system design much simpler and area-efficient [2].

The technical requirements for a wireless interconnect are specified by several conditions. First, the whole transceiver circuitry including the antennas must be integrated within the chip. Second, wireless link must provide sufficient bandwidth for fast enough communication. And third, the range of the link should be very short—a distance of several centimetres is to be covered. Therefore a suitable carrier frequency in the millimetre range can be used to design good chip-to-chip wireless link. The RF circuitry required for the transceivers can be readily implemented even in 90 nm CMOS technology [3], [4], the small wavelength allows for on-chip antenna integration and the high frequency allow for higher absolute bandwidth and therefore higher data rates.

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There are two main problems in integrating the antenna within a CMOS chip. First is the area covered by the antenna. Normally this area is several square millimetres, which is unacceptable by integrated circuit manufacturers. The second problem is the antenna radiation efficiency. The silicon substrate used in CMOS technology is lightly p^- doped, which decreases its resistivity to several Ohm.cm. The electromagnetic field within such substrate is subject to heavy dielectric losses due to this low resistivity, which reduces the antenna efficiency.

The first of these two problems can be tackled by double using available metallisation structures on the integrated circuit. For example the chip ground supply planes can simultaneously serve as antenna electrodes [5]–[7]. This has been achieved by cutting the top metallisation layer into patches and feeding the RF signal across the gap between the patches.

The efficiency of the integrated antenna can be optimised by two methods. One is to use high-resistivity substrate [6]. A drawback of this method is that the thermal conductivity of the substrate is also reduced and this changes the standard CMOS technology. Another interesting option, presented in detail in the current work, is to use very thin substrates. Current technologies like the ChipFilm technology, developed by the Institute for Microelectronics in Stuttgart, Germany, offers the possibility to fabricate integrated circuits on substrates as thin as 6 μm [8]–[10]. Such a substrate increases the antenna efficiency by reducing the volume where the electromagnetic field is subject to a loss. A drawback of this solution is the introduction of several additional steps to the standard CMOS technology.

II. Antenna Mode

A cross-section view of the integrated antenna using the circuit ground plane as electrodes is presented in Fig 1. The antenna is fabricated either on high-resistivity (about 1 kΩ.cm) substrate with thickness of 675 μm, or on thin low-resistivity substrate, as discussed in the previous section. The active elements are fabricated atop the substrate. Several metallisation layers follow, where the on-chip interconnects are fabricated. The top metallisation layer holds the ground supply plane. This plane is cut into patches and an RF generator is connected across the resulting gaps, exciting the antenna.

Since the patches serve as ground planes also for the power supply for the CMOS circuitry underneath them, a low-frequency galvanic connection must be provided between them. The block inductors, providing a DC connection between the patches are not shown in the figure.

The antenna structure consists of two or more patches, separated by narrow gaps. If the length of the gaps is comparable with the wavelength, they can be treated as slot lines. If these

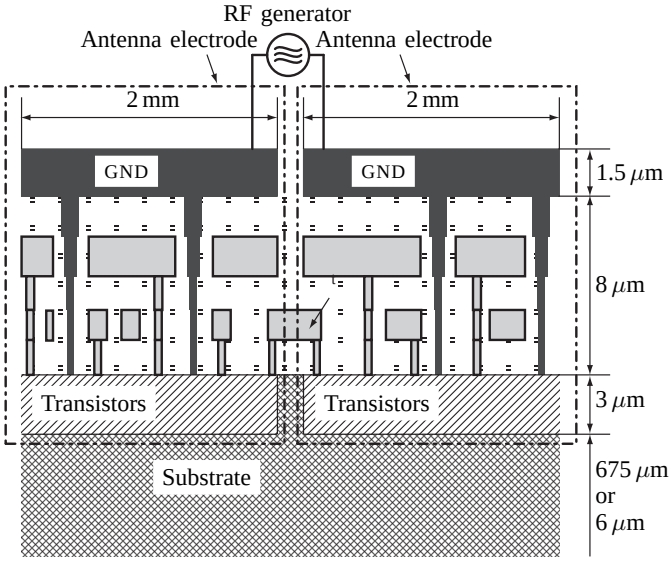

Fig. 1. Detailed view of the cross-section of the integrated on-chip antenna, using the ground planes as antenna electrodes. The separated areas of the ground planes have to be connected to each other using inductive connections. The RF generator is also integrated in the CMOS circuit. Figure is not to scale.

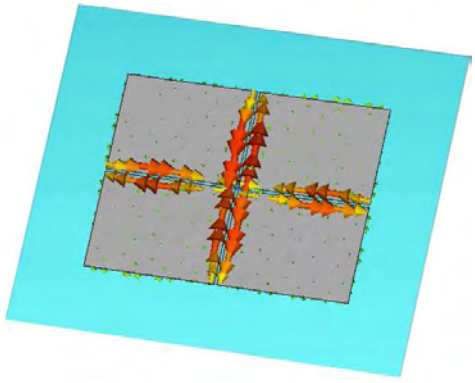

Fig. 2. Current distribution in an 2×2 patch antenna configuration.

lines are terminated with a open or short-circuit, a standing wave pattern will be formed along the line. This standing wave provides a time-varying electric polarisation, which is a source of radiation [11]. Figure 2 shows the current distribution in a four-patch antenna configuration.

The guided wavelength in a slot line is given by [12]

$$\lambda_g = \frac{\lambda_0}{\sqrt{\frac{1}{2}(\varepsilon_{\mathrm{r,Si}} + 1)}}, \qquad (1)$$

where λ_0 is the free-space wavelength and $\varepsilon_{\mathrm{r,Si}}$ is the relative permeability of the substrate. For a carrier frequency of $f = 60\,\mathrm{GHz}$ the corresponding wavelength is $\lambda_g = 1.8\,\mathrm{mm}$. Therefore an open-circuited slot 1.35 mm long is a $3/4\lambda_g$ resonator. Simulations of a two-patch structure, presented in Fig. 3 show that the length of the slot should be a bit shorter, namely 1.1 mm, accounting for the effective slot elongation due to the stray capacitance of the open slot line end. The current distribution, plotted in the figure, shows variation in the current density along the gap.

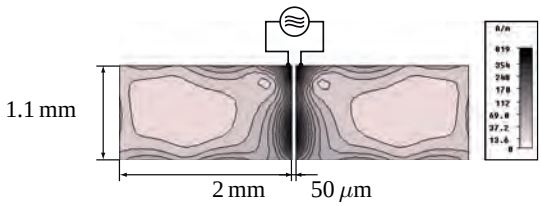

Fig. 3. Top view and current distribution of a two patch antenna, operating at 66 GHz.

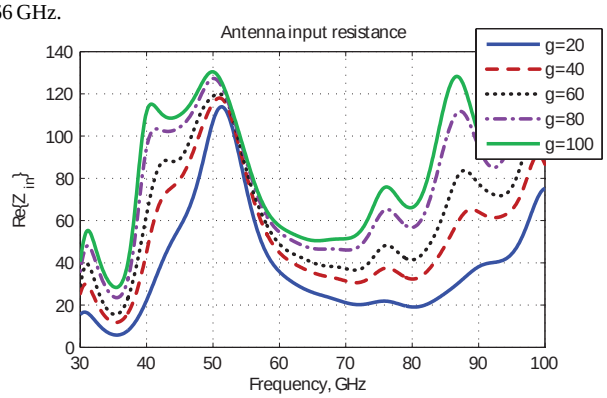

Fig. 4. Real part of the input impedance of the antenna from Fig. 3 for different slot widths g.

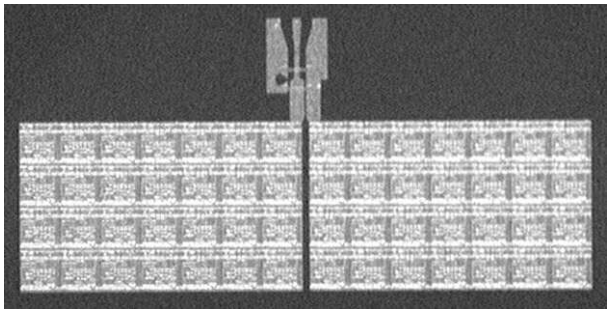

Fig. 5. Photograph of the manufactured antenna.

The input impedance of the antenna depends on the gap width. A plot of the real part of the two-patch slot antenna from Fig. 3 is shown in Fig. rin. The input resistance is smaller for a narrower slot.

The antenna has been manufactured on high-impedance substrate. A photograph of the structure is shown in Fig. 5. The results of the investigation of that type of antennas are presented in [5], [6].

III. Antennas on Thin Substrate

The ChipFilm technology provides the possibility of manufacturing integrated circuits on substrate with thickness as low as $6\,mu$m, as discussed in the introduction. Numerical experiments have been performed to assess the radiation efficiency of antennas on thin substrate.

The antenna loss and the antenna radiation are both modelled as resistors connected in series in the equivalent circuit of the antenna. Therefore it is not possible to identify the antenna efficiency by investigation of the input impedance. The efficiency can be computed numerically by comparing the quality factor of a lossless antenna model and the one of

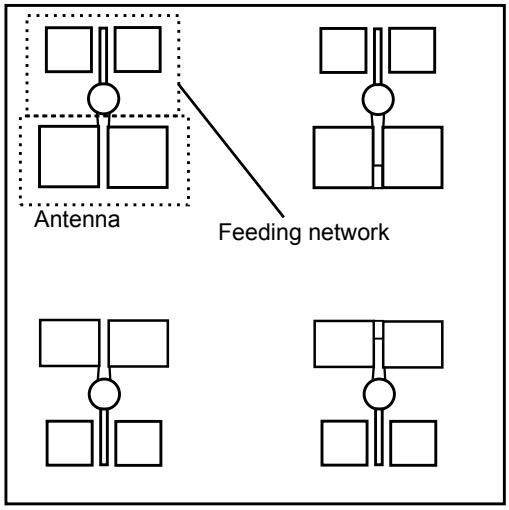

Fig. 6. A top view of the experimental setup.

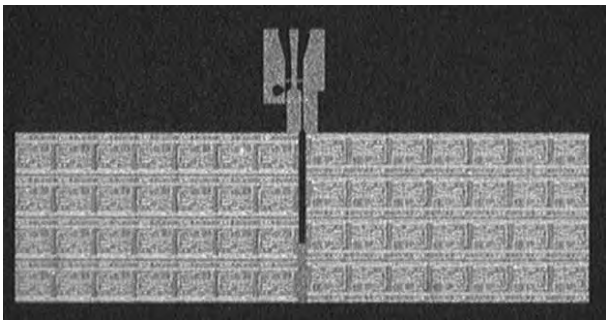

Fig. 7. A photograph of a short-circuited antenna.

a lossy antenna. The quality factor of any two-port is defined as

$$Q = \frac{P_{\text{Active}}}{2\pi E_{\text{Stored}}} = \frac{1}{\Delta f}, \tag{2}$$

or as a ratio between the active input power to the stored energy per cycle, which is inversely proportional to the $-3\,\text{dB}$ bandwidth. Since the antenna input power is the sum of the radiated power and the power lost as heat, or

$$P_{\text{Active}} = P_{\text{rad}} + P_{\text{loss}}, \tag{3}$$

and the antenna efficiency is the ratio of the radiated to the input power,

$$\eta_{\text{Ant}} = \frac{P_{\text{rad}}}{P_{\text{Active}}}, \tag{4}$$

we can compute the antenna efficiency as the ratio of the $-3\,\text{dB}$ bandwidth of a lossless and a lossy antenna,

$$\eta_{\text{Ant}} = \frac{\Delta f_{\text{lossless}}}{\Delta f_{\text{lossy}}} \tag{5}$$

The simulation results show antenna efficiency of $\eta_{\text{Ant}} = 74.8\,\%$. A plot of the return loss of the lossy antenna is shown in Fig. 8.

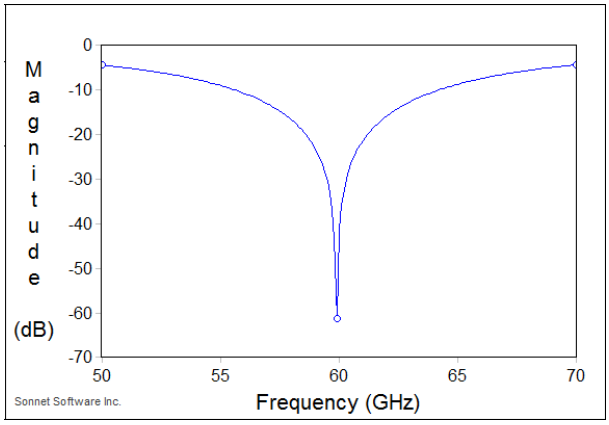

Fig. 8. Return loss of the lossy integrated antenna.

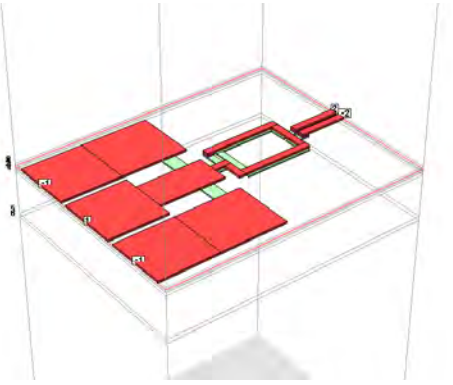

Fig. 9. A 3D model of the balun transformer.

IV. Experimental Setup

The model of antennas on thin substrate is to be verified by measurement. An experimental setup is prepared, which allows the measurement of the input impedance of the slot antenna. The setup contains four antennas, each equipped with a feeding network, as shown in Fig. 6. There are two types of antennas that will be investigated. The first type is the slot antenna, described in the previous section. The second type is the same slot antenna, but short-circuited at the end. Such a short-circuit provides a DC connection between the two patches, as they need to serve as a CMOS circuit ground plane. A photograph of such antenna is shown in Fig. 7. Various antenna lengths for both antenna types have been designed.

The feeding network contains a balun transformer, as the antenna is symmetrical, so that the feeding line should be balanced, whereas the measurement equipment provides unbalanced port connections. The balun is designed using a transformer. The offered technology provides two metallisation layers, so a stacked transformer design has been selected, as the stacked transformers provide lower insertion loss than the single-layered ones [13]. Figure 9 shows a 3D model of the designed balun.

The calibration of the measurement system must be performed using the Throuh-Reflect-Line (TRL) [14] technique in order to de-embed the balun characteristics from the measurement results. This technique allows the calibration of

two-port measurement systems using three different, but not standardised, port loads: direct connection of the measurement ports at the reference plane (Through), connection of high-reflection-factor load (Reflect) and connecting the ports with a short line (Line).

Therefore calibration structures have also been designed on a different chip. The structures allow for the measurement of the input impedance of the antennas at their input ports, while de-embedding the influence of the balun transformers.

V. Summary

This work discusses the design of on-chip integrated antennas with high radiation efficiency and low area requirements. There are two possibilities for minimising the antenna losses—one is using high-resistivity substrate and the other is using very thin substrate. An experimental setup has been prepared to verify the characteristics of integrated antennas on thin substrate. The antenna input impedance and radiation efficiency have been computed.

Acknowledgement

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