Different Implementations of Serial Pseudorandom/Natural Code Converters

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Abstract – ***The duration of the pseudorandom/natural code conversion is critical for the absolute position measurement cycle when pseudorandom position encoders are applied. Because of their simplicity, serial code converters have advantages in implementation. This paper presents serial pseudorandom/natural code converters and proposes one new faster converter. Concrete examples for the proposed solution are also presented.***

Keywords – ***position measurement, pseudorandom position encoder, serial pseudorandom/natural code converter***

I. INTRODUCTION

The pseudorandom position encoders, their main advantage, have only one code track regardless to the resolution. This solution for the absolute position measurement is based on property of n-bit pseudorandom binary sequence (PRBS) that each sliding window of length n, which passed along a sequence, will extract unique code word in every moment [1]. Also, the last (n-1) bits of the current code word are equivalent to the first (n-1) bits of the subsequent code word. The PRBS is useful type of periodic signal and also has the following properties: the signal is periodic and bipolar, signal exhibits a uniform power spectral density over a wide frequency band, signal is deterministic repeatable, etc. Pseudorandom binary sequences are also used in cryptography, bit-error-rate measurements, wireless communication systems, audio applications, etc. The PRBS generator can be implemented using discrete electronics (shift register with D flip-flop cells), using a microprocessor (flexible implementation), using a FPGA-based implementation (flexible and very fast), using virtual instrumentation concept [2], etc.

The main functional parts of pseudorandom position encoder are the code reading system [3, 4], where different solutions are developed (with one, two or more heads), code scanning methods in the sense of reliable code reading moment defining [4, 5], and error detection methods [3], which increase reliability of encoder. One more functional part of encoder, but no less important than previous ones, is pseudorandom/natural code conversion. Pseudorandom binary code is not suitable for direct application in digital electronics. There are different methods for pseudorandom/natural code conversion, and they can be separated on three distinct groups: parallel [6], serial [4] and serial–parallel code conversion [4]. Parallel solution for code conversion is fast, but expensive and impractical for long PRBS. Serial code conversion is developed as one simple and cheap way for conversion of long PRBS. However, conversion time is critical for one absolute position measurement cycle. Through development of different solutions of serial code converters the main goal is reducing of conversion time. Serial–parallel code conversion is one compromise solution, which combines serial and parallel conversion techniques. During mounting on the shaft pseudorandom encoder provides possibility of direct zero position adjustment without a significant change of hardware and software, but only when serial code conversion is used [7].

In the first part of the paper existing serial pseudorandom/natural code converters are explained, and then on new faster serial converter is proposed. This new solution employed different feedback configuration of logic gates. The presented solutions are detailed explained using appropriate concrete example.

II. THE SERIAL PSEUDORANDOM/NATURAL CODE CONVERTERS

The simple solution for pseudorandom/natural code conversion is the serial or sequential pseudorandom/natural code conversion method [4], but in the case of high resolution, the conversion time becomes a limiting factor. This method finds the actual value of the position 'p' simply by counting the steps that the shift register with inverse feedback needs until it reaches the initial state by successive shifting from the read pseudorandom n-bit word. Serial pseudorandom/natural code conversion process for n = 7 is shown in Fig. 1. Pseudorandom code on the code track is read using of only one code reading head $x(7)$ [4]. In the code conversion process one Fibonacci generator with inverse feedback configuration is applied (Fig. 1). The Fibonacci implementation consists of a shift register in which a exclusive-OR (XOR) gates for modulo-2 sum of the binary-weighted taps are used for feedback configuration. The states of the shift register are actually sequential code words of pseudorandom binary sequence until it came to the state that corresponds to the initial code word. The forbidden state is usually referred to be 0000000, because when all the flip-flop

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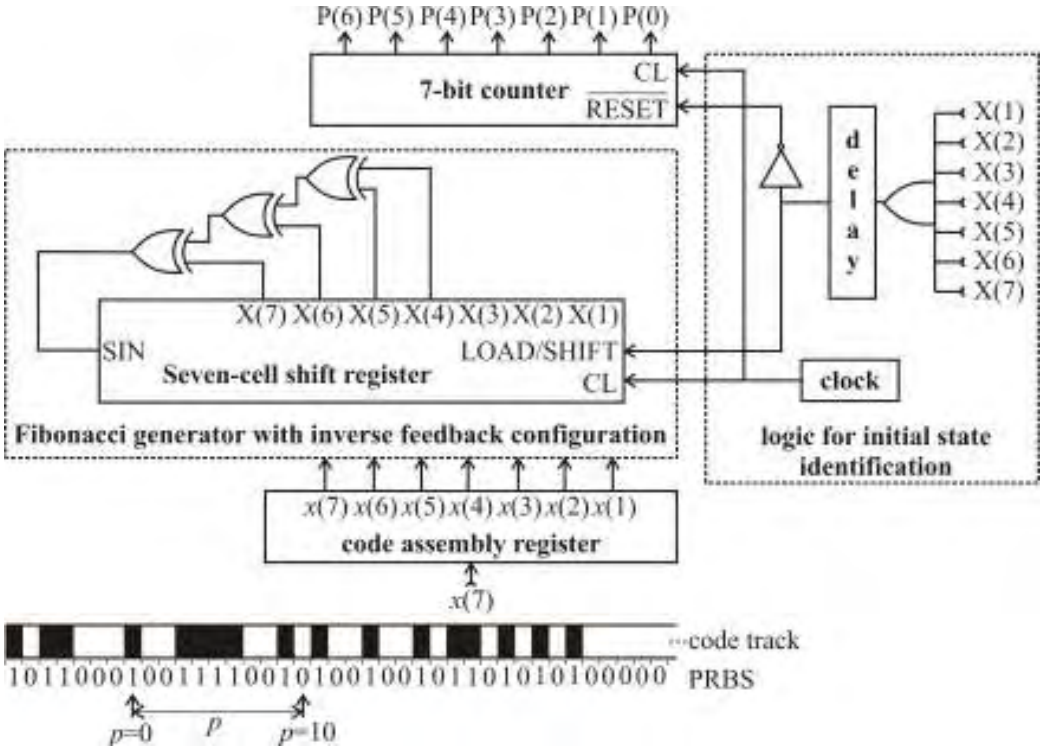

Fig. 1. Serial pseudorandom/natural code converter based on Fibonacci implementation

values are 0, the XOR will reveal a 0 regardless of the location of the taps. Therefore, the fed back value is always 0, and the shift register stays in the 0000000 state. If one of the feedback values are inverted, or XNOR instead XORs are used, the forbidden state may be altered.

Also, in the serial pseudorandom/natural code converter one 7-bit counter is added that counts steps and also the logic for the initial state identification. The basic advantage of this code converter is simplicity, and the disadvantage is the serial connection of logical elements (XOR gates) in the feedback configuration, which increases the total propagation delay and thus conversion time is limited. On the other hand, the conversion time limits the maximum rotation speed of the encoder. The table which contains for maximal length pseudorandom sequences feedback sets for different shift register sizes is given in [2, 8].

One way of reducing the code conversion time of the previous method approximately two times is based on the idea that, thanks to PRBS cycling property, the initial state could be reached using feedback sets that are used for either "direct" or "inverse" PRBS generating [9]. Depending on the previous position of the movable system it is decided which PRBS generating low ("direct" or "inverse") would be used for current code conversion.

Another solution for code conversion process is using the Galois implementation of PRBS generator, which consists of a shift register, the content of which is modified at every step by a binary-weighted value of the output stage, using XOR gates. The pseudorandom binary sequence generator with a parallel feedback logic configuration (Galois generator of pseudorandom binary sequence) is known as a faster pseudorandom binary sequence generator [10]. The Galois generator is generally faster than the Fibonacci in hardware due to the reduced number of logic gates in the feedback loop. Now, the total propagation delay in the feedback configuration is equal to the propagation delay of only one logical gate. The order of the Galois weights is opposite that of the Fibonacci weights, for given identical feedback set. The pseudorandom/natural code converter based on the Galois generator is shown in Fig. 2. It is added a logic that the read code word converts to the appropriate content of the shift register. When the code word is read, this logic provides the equivalent state of the shift register that is loaded in that shift register. This logic does not participate further in the code conversion process and thus negligibly influences to conversion time. Furthermore, the steps counted that are needed for the shift register with the determined and the written state come from the known initial state of the shift register. The obtained number is the result of the conversion, the same as in the case of the known serial code converter (Fig. 1). In the second part of the paper the proposed logic for translation of the read code word in the appropriate content of the shift register is explained in detail, without which it would not be possible to realise the new code converter.

III. Logic for initial adjustment of read pseudorandom code word

The read n-bit pseudorandom code word (assigned as $x = x_n x_{n-1} x_{n-2} \ldots\ldots x_2 x_1$) in real time is not identical to the n-bit current content of the shift register (assigned as $X = X_n X_{n-1} X_{n-2} \ldots X_2 X_1$), which corresponds to the position of this code word in the generated pseudorandom binary sequence. For each n-bit code word of the pseudorandom binary

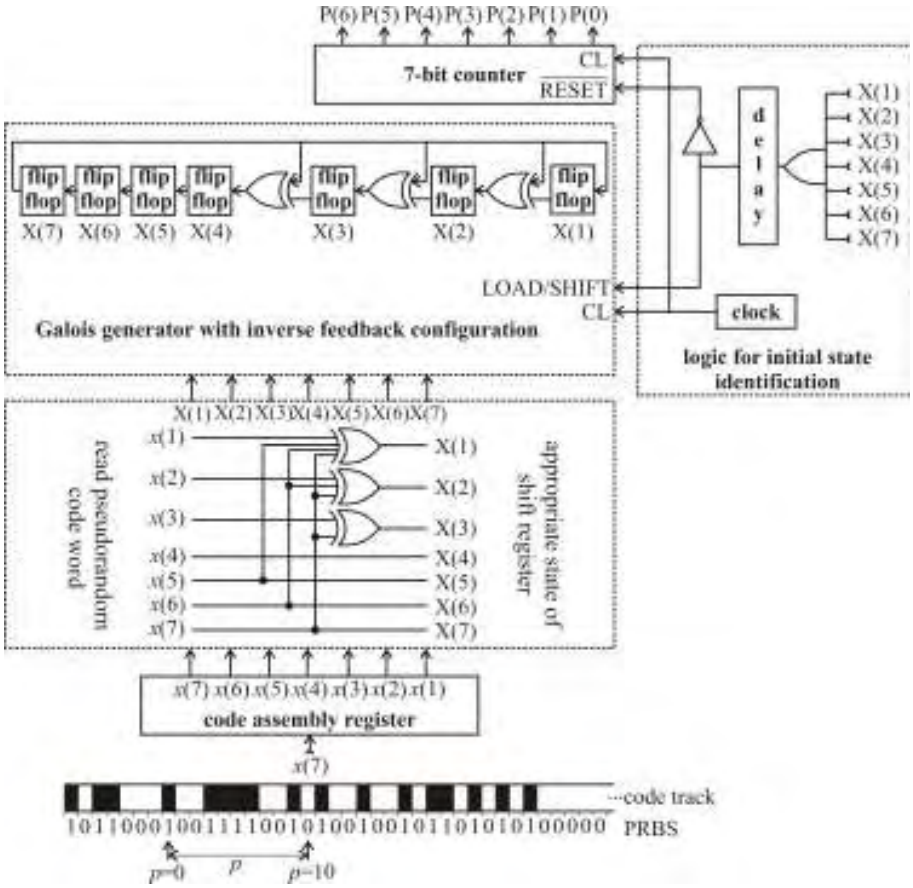

Fig. 2. Faster serial pseudorandom/natural code converter based on Galois implementation

sequence there corresponds exactly one state of the shift register with a parallel feedback logic configuration and it is possible to design a simple logic composed from XOR gates (Fig. 2). For $n = 7$ will be shown process of logic design, and such a procedure is applicable to any other pseudorandom binary code word of arbitrary length. On the Fig. 3 is shown passing through the states of the 7-bit shift register with a parallel feedback logic, which is known as a 'Galois' shift register [8, 10]. On the start, suppose that the initial content of the shift register is $\{X_1, X_2, X_3, X_4, X_5, X_6, X_7\}$ and the pseudorandom code word $\{x_1, x_2, x_3, x_4, x_5, x_6, x_7\}$ corresponds to that content. The direct generation law of PRBS and the moving direction from X_1 to X_7 is applied. The pseudorandom bit output is always identical to the state X_7, and

$$X_7 = x_7 \tag{1}$$

After the first clock pulse, the content of the shift register becomes $\{X_7', X_6', X_5', X_4', X_3', X_2', X_1'\}$, where, in accordance with the direct generation law of pseudorandom binary sequences for $n = 7$:

$$\begin{aligned} X_7' &= X_6 \\ X_6' &= X_5 \\ X_5' &= X_4 \\ X_4' &= X_7 \oplus X_3 \\ X_3' &= X_7 \oplus X_2 \\ X_2' &= X_7 \oplus X_1 \\ X_1' &= X_7 \end{aligned}$$

The relations for the parallel feedback logic configuration are well known, based on the known serial feedback logic configuration of the n-bit shift register [8]. According to basic mathematical relationships $X_7' = X_6$, and $X_7' = x_6$, can be concluded

$$X_6 = x_6 \tag{2}$$

Then, after the second clock pulse the content of the shift register becomes $\{X_7'', X_6'', X_5'', X_4'', X_3'', X_2'', X_1''\}$. According to previous principle the following relations are obtained:

$$\begin{aligned} X_7'' &= X_6' \\ X_6'' &= X_5' \\ X_5'' &= X_4' \\ X_4'' &= X_7' \oplus X_3' \\ X_3'' &= X_7' \oplus X_2' \\ X_2'' &= X_7' \oplus X_1' \\ X_1'' &= X_7' \end{aligned}$$

Since $X_7'' = x_5$ and $X_7'' = X_6'$, plus from the previous clock pulse the valid relation is $X_6' = X_5$, there is obtained

$$X_5 = x_5 \tag{3}$$

With the identical procedure for the next clock pulse or by writing the relations on the same principle and using the relations from the previous clock pulse, and also properties of modulo-2 sum, the following dependences are obtained:

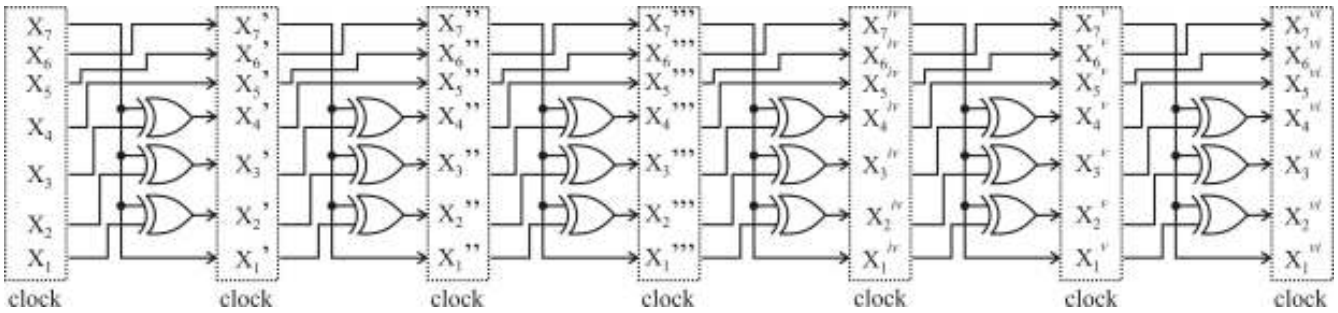

Fig. 3. Contents of the 'Galois' shift register through 7 clock periods

$$X_4 = x_4 \quad (4)$$
$$X_3 = x_3 \oplus x_7 \quad (5)$$
$$X_2 = x_2 \oplus x_6 \oplus x_7 \quad (6)$$
$$X_1 = x_1 \oplus x_5 \oplus x_6 \oplus x_7 \quad (7)$$

These seven relations define relations between the content of the register and the appropriate pseudorandom binary code word, and also define the logic for initial adjustment of the read pseudorandom binary code word shown in Fig. 2.

Now compare the conversion of the read pseudorandom code word {0, 1, 1, 0, 0, 0, 1} for the case of applying the first explained serial code converter and the proposed faster serial code converter. The initial code word is {1, 1, 1, 0, 0, 1, 0}. According to the algorithms described in [4], the pseudorandom/ natural code conversion is accomplished sequentially after loading it into a shift register having a reverse feedback equation $X(1) = X(4) \oplus X(5) \oplus X(6) \oplus X(7)$ (Fig. 1). In the given example there are 10 shifts of register, and the counter state is $p = 10$ at the end, which is actualy the value of the current position of the movable system. Let us now look at the new code converter, which is shown in Fig. 2. The code track is the same as shown in Fig. 1. Now, the read code word is not written directly to the shift register, but feds the input of logic for the initial adjustment of the read code word (Fig. 2). By the application of relations (1), (2), (3), (4), (5), (6), (7) the code word {0, 1, 1, 0, 0, 1, 1} is obtained as output. It is now directly saved in the shift registry. Now, the shift register sequentially passes through the following states: {1, 1, 0, 0, 1, 1, 0}, {1, 0, 0, 0, 0, 1, 1}, {0, 0, 0, 1, 0, 0, 1}, {0, 0, 1, 0, 0, 1, 0}, {0, 1, 0, 0, 1, 0, 0}, {1, 0, 0, 1, 0, 0, 0}, {0, 0, 1, 1, 1, 1, 1}, {0, 1, 1, 1, 1, 1, 0}, {1, 1, 1, 1, 1, 0, 0}, and {1, 1, 1, 0, 1, 1, 1} when the stop will be. The state {1, 1, 1, 0, 1, 1, 1} is the content of the register, which corresponds to the initial pseudorandom code word {1, 1, 1, 0, 0, 1, 0}. So, at the end of conversion the counter state is $p = 10$, which is exactly the same value as in the case of the first serial code converter.

IV. Conclusion

During development of this faster serial pseudorandom/nature code converter the goal was to reduce the conversion time. It is achieved by the reduction in the number of serial connected gates in the feedback logic, which provides less propagation delay. For implementation of code converter, the parallel feedback logic configuration is applied and there has also been designed a simple logic of initial adjustment of the read code word into a appropriate state of the shift register, without which it would not be possible to realise the code converter proposed here.

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