A Proposal for Harmonic Rejection Mixer Avoiding Irrational Weighting Ratios

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Abstract – **A harmonic rejection mixer (HRM) suitable for SDR/CR applications is proposed. Two main difficulties in HRM realization are addressed: The necessity to use irrational weighting ratios and the need of a clock frequency, which is a multiple of the desired LO frequency. In the proposed HRM the first not rejected harmonic is 7-th harmonic. Instead of being 8, as in a comparable traditional HRM, the clock division ratio here is 3 and no weighting is used.**

Keywords – **harmonic rejection mixer, receiver front-end, software receiver.**

I. INTRODUCTION

Due to the nonlinearity of the mixer and the presence of higher harmonics in the waveform of the local oscillator (LO), the heterodyne receivers are susceptible to interference from signals present at $f = nf_{LO} \pm f_i$, where f_i is the intermediate frequency (IF) used. In traditional receivers, high-order preselect filters are used to solve this problem. However, such filters are difficult or impossible to integrate on-chip and are space and sometimes power consuming. Therefore, it is desirable to relax the RF filtering requirements as much as possible.

A key requirement for software radio receivers, especially for cognitive radio applications is the ability to cover a wide frequency range. In such cases using a square wave LO is preferable to sinusoidal, since the wide range of LO frequencies needed, can be easily produced in an IC by means of a PLL synthesizer with a relative narrow frequency range which is combined with digital frequency dividers. However, the square LO waveform contains strong harmonics and this exacerbates the requirements to RF filtering.

Another popular solution when designing receiver ICs, especially zero-IF receivers, is to use passive switching mixers because of their better linearity, nearly zero power consumption, and lower 1/f noise [1]. But, the use of such mixers also adds up to the RF pre-filtering requirements.

The RF filtering requirements can be significantly relaxed when a harmonic rejection mixer (HRM) is used. In a HRM some unwanted mixing products can be cancelled [2]. A HRM (Fig. 1) consists of several switching mixers driven by separate LO square waves with different phases or duty cycles. The input signals for the individual mixers are delivered by separate RF preamplifiers with weighted gains. The individual mixer outputs are connected in parallel. Such a HRM is equivalent to a single mixer, driven by an effective

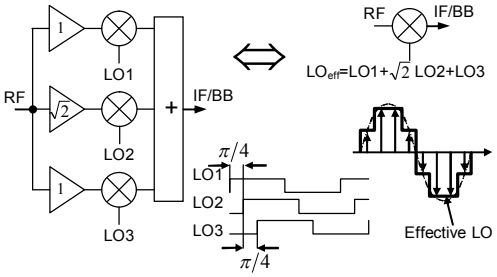

Fig. 1. A typical harmonic rejection mixer

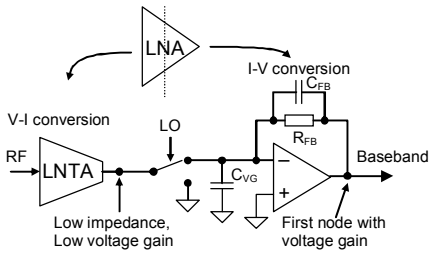

Fig. 2. Conceptual diagram of low-pass blocker filtering [3]

LO waveform in which some harmonics are removed. The LO waveform is in fact a weighted sum of the individual LO waveforms. In HRM, which have been proposed up to now, the effective LO waveform is based on a uniformly sampled sinusoid.

Relaxed RF filtering imposes increased requirements on the LNA and the mixer linearity in the presence of strong interferers. This is a very serious concern especially in receiver IC design, due to the current trend of decreasing supply voltages and the corresponding reduction of voltage headroom.

A successful solution of this problem is presented in [3], in which an integrated CMOS zero IF receiver front-end, using a HRM in conjunction with a well-devised architecture, is proposed. A conceptual block diagram of this receiver is presented in Fig. 2. Voltage amplification in a LNA is usually realized using voltage-to-current conversion via a transconductance followed by current-to-voltage conversion via some impedance or transimpedance. In the proposed receiver, the passive mixer is inserted between a low-noise transconductance amplifier (LNTA) and the virtual ground node of a transimpedance amplifier (TIA). Due to the RC network in its feedback loop, it also acts as a LPF. The mixer load impedance is maintained low in a wide frequency range, which leads to a low LNTA load impedance, too. Thus, large voltage swings at the LNTA output and in the mixer are avoided. The first voltage gain occurs at baseband after the low-pass filtering, where the out-of-band interferers are significantly attenuated.

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A serious difficulty in HRM realization is the need of irrational weighting ratios. The required ratios have to be approximated by rational numbers, which leads to some errors, resulting in worsening the harmonic rejection (HR).

Another difficulty is the need of a multiphase LO. This can be realized by shift registers (SR) or using a delay locked loop (DLL) with a tapped delay line. The DLL implementation is disadvantageous due to the phase noise amplification in the DLLs [4] and the phase noise accumulation from one delay cell to the next one along the delay line [5]. A serious disadvantage of the SR implementation is its frequency dividing nature. If the first harmonic that is not rejected is *n*-th, a LO with (*n*+*1*) phases is required. In this case a clock frequency $f_{CLK} = (n+1) f_{LO}$ is needed.

It is clear by intuition that the values of a uniformly sampled sinusoid are related by irrational ratios. However, it is interesting to see whether there are special cases where the ratios in question are rational. We examined this problem and proved (see the Appendix) that the irrational ratios can be avoided only when the number of samples per period is not greater than 6. Therefore, another approach to harmonic rejection is desirable.

The purpose of this work is to develop a HRM in which the above mentioned problems are mitigated. This can be done at the cost of some HR degradation at the highest frequencies received. However, harmonic mixing is not such a serious concern at those frequencies.

The rest of the paper is organized as follows. Section II describes the proposed approach to harmonic rejection and the considerations related to the practical implementation of HRM based on this approach. Section III gives the simulation results.

II. HRM APPROACH PROPOSAL

Generally, a periodic pulse train with a frequency $f = 1/T$ contains components at all possible multiples of f including DC. In the case of rectangular pulses, the components with frequencies of n/T_P will be zero. If a copy of this pulse train is shifted by π and subtracted from original pulse train, all even harmonics and the DC component will be canceled. If a copy of the resulting waveform is shifted by $\pi/3$ and added to it, all harmonics of orders $3(2n+1), n = 0,\ 1,\ 2,\ 3,...$ will be canceled (see Fig. 3) and so on. Mathematically this can be described by following recursive formula:

$$p_0(t) = \mathrm{rect}(t/T_P) \otimes [\delta(t) - \delta(t - T_{LO}/2)] \otimes \sum_{n=-\infty}^{\infty} \delta(t - nT_{LO})$$

$$p_{i+1}(t) = p_i(t) + p_i(t) \otimes \delta[t - T_{LO}/(2h_{i+1})],$$

where h_{i+1} is the order of harmonic canceled by the current addition. Fourier series coefficients will be:

$$C_{n0} = \frac{T_P}{T_{LO}} \mathrm{sinc}\left(\pi n \frac{T_P}{T_{LO}}\right) \cdot \left[1 - (-1)^n\right] \text{ and}$$

$$C_{k(i+1)} = C_k \left(1 + e^{-j\pi n/h_{i+1}}\right).$$

No weighting is needed. A drawback of this approach is that the complexity doubles for each additional rejected group of harmonics. It seems that this approach can be applied for the cancellation of harmonics up to 7th order.

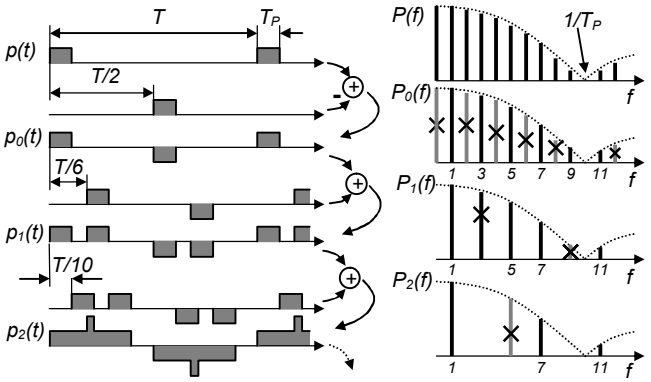

Fig. 3. Illustration of proposed HR approach

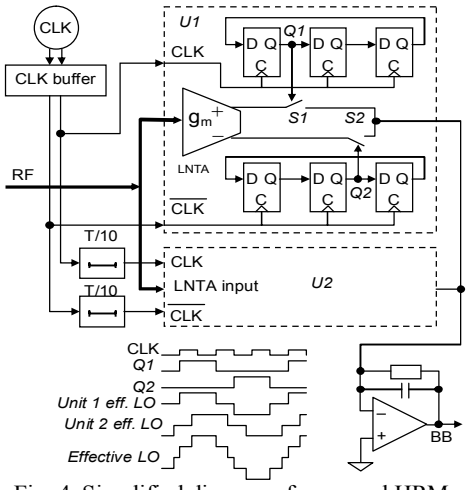

Fig. 4. Simplified diagram of proposed HRM

All the necessary time intervals can be obtained using some form of frequency dividers (e. g. shift registers). A drawback of this technique is the need of a clock frequency, which is a multiple of the LO frequency. Alternatively, delay cells can be used. However, delay cells increase the jitter variance roughly proportionally to the implemented delay [5]. Therefore, it is desirable that the largest delays are to be implemented without using delay cells.

Fig. 4 presents a simplified block diagram of HRM based on above considerations. The first harmonic that is not canceled is the 7th harmonic. The mixer is involved in a receiver architecture similar to the one described in [3]. The mixer contains two identical units - U1 and U2 – each one having two SRs with "100" bit patterns circulating. As a result, the pulse width at the flip-flop outputs is $T_{LO}/3$. Hence, the harmonics of orders $3n$ are suppressed. The switches S1 and S2, connected to the direct and inverse outputs of the LNTA respectively, are controlled by pulses spaced at $T_{LO}/2$. As a result, all even harmonics are cancelled. By adding the U1 and U2 output currents at the virtual ground node of the TIA, the harmonics of orders $5(2n+1)$ are canceled. Additional switches can be controlled by the unused shift register outputs and used to obtain three effective LO spaced at $2\pi/3$. We designate them as R, S and T.

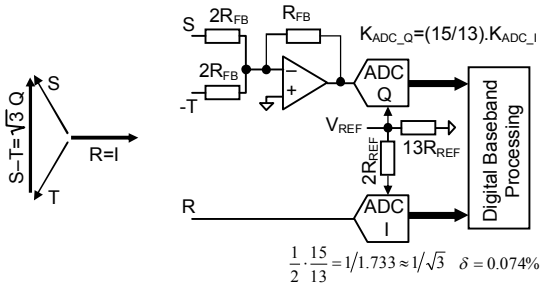

Fig. 5. Obtaining quadrature BB signals

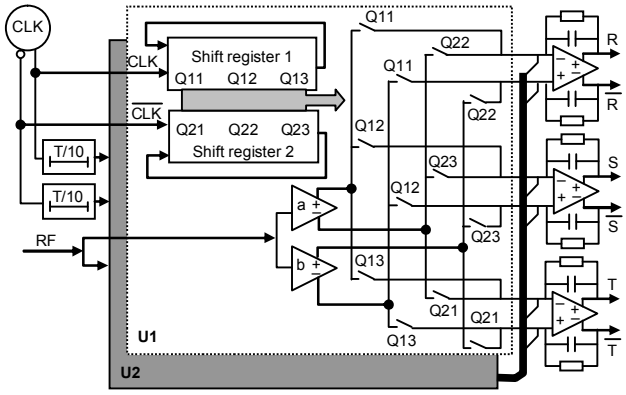

Fig. 6. Proposed HRM

Such a HRM appears to be unable to provide quadrature baseband output signals. A possible solution of this problem is suggested in [6]. We propose a simpler solution illustrated by Fig. 6.

A possible practical implementation of this HRM is presented in Fig. 6. The mixer consists of two identical units again. Each unit has two identical LNTAs. Special attention has been paid to the LNTA output assignment in order to minimize harmonic rejection worsening due to amplitude mismatches. It can be seen that when one input of some of the TIAs is connected to the direct output of a certain LNTA, the opposite input of the same TIA is always connected to the inverse output of the other LNTA. This reduces the influence of LNTA transconductance mismatches on the half-wave symmetry of the effective LO waveforms. Thus, the sensitivity of the even-order HR to LNTA mismatches is reduced.

Quadrature baseband signals can be obtained according to the way shown on Fig. 5. However, it is possible to perform the necessary subtraction directly at the virtual ground node of one of the TIA. In this way the third TIA and the summing amplifier can be spared. This is worth doing because the transimpedance amplifier occupies a large area on the IC die, as can be seen on the micrograph in [3]. In this case, special care should be taken to avoid the formation of low-ohmic paths in the input of the TIA if on-time overlaps occur during switching (Fig. 7) - an effect leading to a significant increase of the TIA noise [7]. When the zero-crossings of the Q LO waveform occur, the I LO waveform is constant, so two of the LNTA outputs (from a total of 4) are used and are unavailable. Therefore in Q zero-crossing moments when a TIA input is disconnected from a LNTA output, the opposite TIA input will be connected to the same LNTA output. If

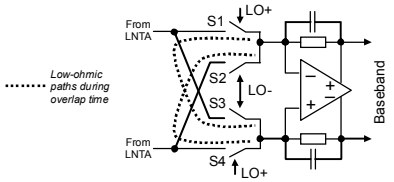

Fig. 7. Low-ohmic paths at the TIA input during on time overlaps

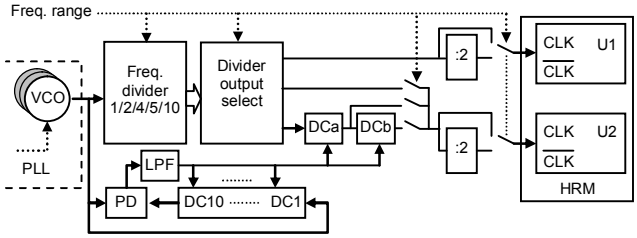

Fig. 8. Clock generation for proposed HRM

there is an on-time overlap, a low-ohmic path between two TIA inputs will arise. Therefore, no LNTA output assignment exists to prevent low-ohmic paths between TIA inputs.

The wide LO frequency range needed is achieved by a PLL synthesizer covering an octave using three VCOs with tuning ranges of about ±12% and frequency dividers. The considerations, leading to this solution, are presented in [8] and [9].

A conceptual block diagram of the CLK generation circuitry is given in Fig. 8. The logical signals are differential, but are presented as single ended for simplicity.

Even division ratios are used only to obtain pulses with a true 50% duty cycle. The latter is important for obtaining high even harmonic rejection ratios. When $f_{LO} > f_{LO\max}/2$ no frequency division is used and we rely solely on the symmetry of the VCOs, therefore even harmonic rejection is poor. However, at the highest receiving frequencies the harmonic mixing presents less concern.

The delay needed for the 5th order HR is implemented by controlled delay cells and an appropriate design of the frequency divider. It can be found out that only two delay values are required - $T_{VCO}/10$ and $2T_{VCO}/10$ - independent of the LO frequency. The corresponding delay cells are connected to appropriate outputs of the divider depending on the VCO division ratio used. When $f_{LO} \le f_{LO\max}/10$, the needed delay value is obtained exactly without using delay cells. The control voltage for the delay cells is produced in a DLL with a delay line consisting of 10 delay cells of the same type as DCa and DCb.

III. RESULTS

Monte Carlo simulations were performed (10 000 runs) to estimate HR worsening due amplitude and phase mismatches. CLK duty cycle error, timing errors due to shift registers and delay cell, as well as amplitude mismatches are assumed to be uncorrelated, normally distributed random variables with standard deviations σ_{DtC}, σ_{ShR}, σ_{DU} and σ_A respectively.

We assumed that $\sigma_{ShR} = 0.08$ ps (as in [3]), $\sigma_{DtC} = 10^{-2} T_{VCO}$

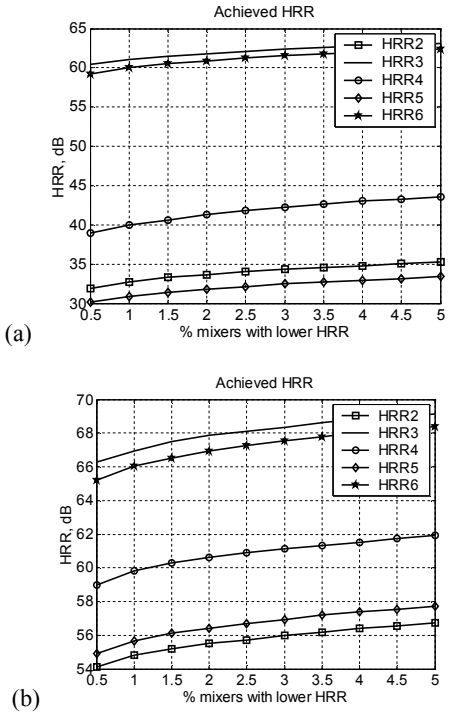

Fig. 9. Achieved HRR, (a) without VCO divider ($f_{LO} > f_{LO\max}/2$), and (b) VCO division ratio 2 , i.e. $f_{LO\max}/4 < f_{LO} < f_{LO\max}/2$.

when $f_{LO} > f_{LO\max}/2$ and $\sigma_{DtC} = 0.08\,\text{ps}$ in the other cases, $\sigma_{DU} = 10^{-2}\tau_{nom}$, and $\sigma_A = 1.10^{-3}$. VCO frequency was 6 GHz.

Fig. 10 shows the HRR versus the percentage of mixers with inferior HRR.

As it was expected, the HRRs worsen significantly for the highest LO frequencies when no frequency divider is used.

For LO frequencies below $f_{LO\max}/2$, the clock signal has a true 50% duty cycle. The latter is essential for the even order HR and 5-th order HR in presented HRM. In addition, relative time errors decrease when the LO period rises. As a result, the HRR's are significantly increased.

IV. Conclusion

A HRM was presented in which no irrational weighting ratios are needed. The clock frequency for up to the 6th order HR is $3f_{LO}$ instead $8f_{LO}$ as in comparable traditional HRM. Additionally, no weighting is used. The penalty is some HR degradation at highest LO frequencies. On the other hand HRR can be significantly improved if a digital cancellation technique is applied, similar to those in [3].

Appendix

We assume that there exist $P \in \mathbf{N}$, $P > 6$ and some phase displacement $\alpha \in (0, 2\pi/P]$, such that $\sin(\alpha + n \cdot 2\pi/P)/\sin(\alpha) \in \mathbf{Q}$ is fulfilled for each $n \in \mathbf{N}$.

If the above statement is true, then it is fulfilled for $n = 1$ and $n = P - 1$ in particular. Therefore, $\sin(\alpha + 2\pi/P)/\sin(\alpha) = \cos(2\pi/P) + \cot(\alpha)\sin(2\pi/P) = k/l$ and $\sin[\alpha + (P-1)\cdot 2\pi/P]/\sin(\alpha) = \sin(\alpha - 2\pi/P)/\sin(\alpha) = \cos(2\pi/P) - \cot(\alpha)\sin(2\pi/P) = p/q$, where $k, l, p, q \in \mathbf{N}$. After summing up the two equations above, we obtain $2 \cdot \cos(2\pi/P) = \frac{kq + pl}{lq}$. Therefore $\cos(2\pi/P) \in \mathbf{Q}$.

According to Niven's theorem [10] if x/π and $\sin(x)$ are both rational, then the sine takes values 0, $\pm 1/2$ and ± 1. We found, that $\cos(2\pi/P) \in \mathbf{Q}$. But $\cos(2\pi/P) = \sin(\pi/2 - 2\pi/P)$. Obviously $(\pi/2 - 2\pi/P)/\pi = (1/2 - 2/P) \in \mathbf{Q}$. Therefore $\cos(2\pi/P)$ can take values 0, $\pm 1/2$ and ± 1. As a result, the minimal non-zero value of $2\pi/P$ is $\pi/3$. Hence $P \le 6$ must be fulfilled contradicting our requirements. Therefore no $P \in \mathbf{N}$, $P > 6$ and $\alpha \in (0, 2\pi/P]$ exist such that $\sin(\alpha + n \cdot 2\pi/P)/\sin(\alpha) \in \mathbf{Q}$ for each $n \in \mathbf{N}$.

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