Different Technological Methods for Offset Compensation in Si Hall Effect Sensors

Ivelina Cholakova[1]

Abstract – **This paper presents technological methods for offset compensation of symmetrical Hall sensors. The offset compensation is one of the most important tasks to solve for accurate measurements by such type of magnetic sensors. The presented methods could be a good solution because the main conductive region is deeply "buried" in the epitaxial layer. In this way it will be away from the surface and well isolated from the substrate modulation.**

Keywords – **Magnetic sensors, Hall effect sensors, offset compensation, CMOS 0.18 µm technology.**

I. Introduction

A Hall element is used for contactless measurement, for example as linear and angular positions, electrical current and power, etc. The Hall element, fabricated by means of CMOS technology gives a weak output signal (of the order of few millivolts). This signal is corrupted of offset and noise [1]. The offset is the output signal of the modulating type of sensor (in most cases with a differential output) in the absebse of an external magnetic field (B = 0). Essentially, this kind of error is a static value or a very slow variation with time of voltage, current or frequency. If there is no additional information concerning the magnetic field or the sensor itself, the offset cannot be distinguished from the useful output signal. If the offset is time invariant, it causes a parallel shift of the whole calibration curve [2]. The offset occurrence is due to several external and internal reasons, as most of them are related mainly to the fabrication process as tolerance of device geometry (for example misalignment of Hall terminals), non-uniform distribution of doping impurities, uneven thickness, crystal damage and dislocations, mechanical stress and strain. Great numbers of methods are utilized in order to reduce or compensate the offset: applying improved fabrication technologies or particular sensor constructions; additional technological treatment of each device; formation of additional control electrodes in the active sensor area, various offset compensation circuits, sensitivity-variation offset reduction method, etc [3].

II. Methods for offset reduction of a Hall effect device

In many applications magnetic sensors are used, e.g. for contactless measurements. Silicon Hall sensors are the prime candidates for such applications due to their cost-effective integration potential. But they have a stress voltage offset which cannot be easily compensated in the production line, so that the offset reduction methods have to be applied [4].

There is a spinning current method which averages the results of several consecutive Hall measurements with different orientations in the crystal plane. Very low residual offsets in the microtesla range can be achieved but the circuitry required may introduce problems [4].

The so called Anti-Hall (AH) method for Hall plates described in [5] also utilizes different orientations in the current injection. The currents are injected at different points but at the same time on the outer and inner boundaries of the sample. Besides the magnetic field sensitive signal, a separate stress sensitive signal can be measured simultaneously at another pair of voltage contacts.

Of course, there are many schematic solutions for offset reduction. The simplest method of offset adjustment is shown in Fig. 1, and uses a manual potentiometer to null out the offset of the Hall effect transducer. The potentiometer is used to set a voltage either positive or negative with respect to the output sense terminal, and a high value resistor sets an offset current into or out of the transducer. It is possible to null out either positive or negative offsets with this scheme.

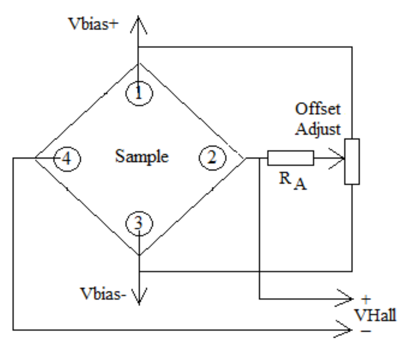

Fig. 1. Manual offset adjustment using potentiometer

A feature of this method is that it can be used regardless of whether the transducer is biased with constant current or a constant voltage source [6].

More complicated method, for example is the dynamic compensation of the offset of an integrated Hall sensor with an instrumentation amplifier. As a result of the interchange of the bias and Hall contacts, Hall voltage remains with the same value and sign, while the offset retains its magnitude, but its sign is reversed. By using the sample & hold technique the signals from each of the two consecutive commutations are added in the signal processing circuit which in essential is a instrumentation amplifier. This approach enables building

[1]Ivelina Cholakova is with the Faculty of Electronic Engineering and Technologies at Technical University of Sofia, 8 Kl. Ohridski Blvd, Sofia 1000, Bulgaria, E-mail: inch@ecad.tu-sofia.bg.

electronic systems for accurate contactless measurements by magnetosensitive device [3].

Another solution, for example, is proposed by Melexis in their Programmable Linear Hall Effect Sensor. CMOS Programmable, Ratiometric Linear Hall Effect sensor IC. The linear output voltage is proportional to the magnetic flux density. The ratiometric output voltage is proportional to the supply voltage. The MLX90251 possesses active error correction circuitry, which virtually eliminates the offset errors normally associated with analog Hall Effect devices. Integrated on the MLX90251 is a temperature-compensated quad switched Hall plate, chopper stabilized amplifiers, adjustable output filter, output driver, voltage protection circuitry and a programmable EEPROM with security and redundancy. Programming the EEPROM allows each device to be calibrated in the application [7].

An alternative to all mentioned methods above, are the technological methods for offset compensation, some of them will be described in the publication with experimental results.

The offset originating from the mask misalignment can be minimized by designing an appropriate layout of the sensor. Also the sensor should be symmetrical for better results. The sensor geometry could also be optimized [1]. One of the proposed methods is the cell to be rotated to 45 degrees in order to orient it along the crystallographic direction (110). It is experimentally proved that in this direction the piezo-resistive coefficient takes the minimum for an N-well Hall device.

A 40um Hall plate was implemented as a basic cell. The layers used in the design are: 3.3V N-well, n-implantation for the contacts, diffusion layer, p-implantation, which is a shallow p+ layer which increases the average resistance and decreases the thickness of the Hall plate. It also acts as an electrostatic shield. The main purpose is to avoid the surface malformations which lead to offset; there is also a metal layer on the top of the Hall sensor which acts as a shield layer. The basic cell is illustrated on Fig. 2.

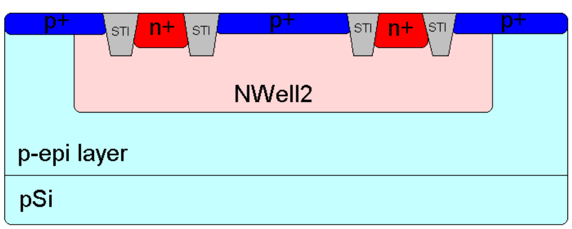

Fig. 2. Hall plate

III. Experimental Results

A test chip was designed with Hall sensors on the XFAB XH018 process. The purpose of this test chip is to test different Hall sensors on the XFAB XH018 technology and to find the optimum Hall sensors for future projects on this technology.

The sensors were tested in order the residual offset to be established. A four-phase spinning method is used with the aim the offset to be cancelled. The test equipment is shown in Fig. 3.

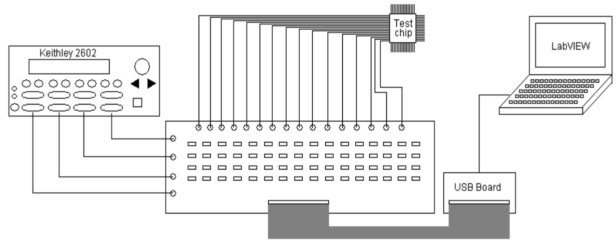

Fig. 3. Test equipment

The equipment is made in order four Hall plates to be tested at once. A LabVIEW program was created for more automated test process. For chip measurements a Keithley 2602 was used which is duo channel source meter with 10,000 readings/s and 5.500 source-measure points/s to memory. One of the channels is used as a source to supply the test chip and the other channel is used to measure the output signal. The plates are tested in six different supply voltages (from 0.5V to 3.00V with step of 0.5V). We also use a Switch Matrix Board with 64 relays which provide the 4-phase spinning method, which in our case is used to cancel the offset (Fig. 4).

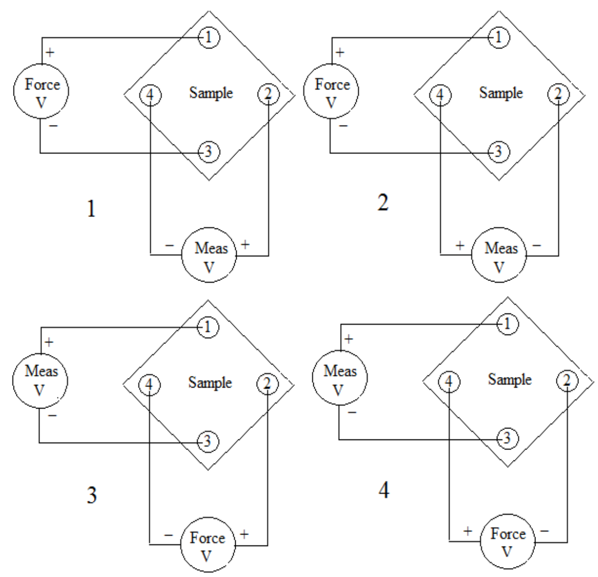

Fig. 4. 4-phase spinning method

The experimental results are shown at Table 1, where the residual offset is in μV and the supply voltage is at Volts. The structure which is examined is designed with shallow trench isolation layer (STI) instead of active area and is shown in Fig. 5.

TABLE I
RESIDUAL OFFSET

Supply voltage, V	Residual Offset, uV	Residual Offset, uV	Residual Offset, uV
0.5	1.8675	1.881	1.147
1	0.7185	0.553	0.054
1.5	0.8275	1.0125	0.7125
2	0.501	1.2865	0.693
2.5	1.9515	1.46	0.926
3	1.9255	1.9745	1.494

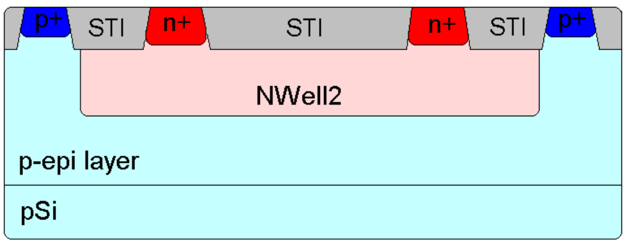

Fig. 5. Hall plate with STI layer

The results present that the worst residual offset is at 0.5V and it is ~ 0.9% of the output signal.

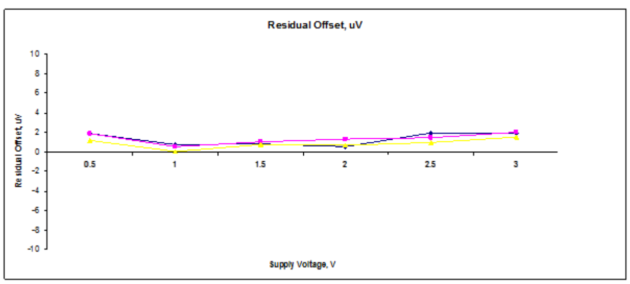

Fig. 4 illustrates three measurements at the same Hall plates under certain conditions. This result is in accordance with the maximum limits for the residual offset and the sensor is appropriate for the applications it is designed, because a high accuracy is required in the automotive industry.

IV. CONCLUSION

In this paper a technological solutions of symmetrical 0.18 CMOS Hall effect sensors for effectively offset compensation are proposed and explained. These solutions effectively improve the stability of the Hall output voltage, because the residual offset, which is inevitable, is optimally reduced.

ACKNOWLEDGEMENT

The research in this paper was carried out within the framework of Contract No. 122ПД0060-03.

REFERENCES

[1] Zoran B. Randjelovic, Maher Kayal, Radevoje Popovic and Hubert Blanchard, *Highly Sensitive Hall Magnetic Sensor Microsystem in CMOS TechnologyHighly Sensitive Hall Magnetic Sensor Microsystem in CMOS Technolog*, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 37, NO. 2, pp. 151-159, 2002.

[2] C. S. Roumenin, *Solid State Magnetic Sensor*, HANDBOOK OF SENSORS AND ACTUATORS, Volume 2, Elsevier, 1994.

[3] Kamen Fillyov, Tihomir Takov, Tzvetelina Tzeneva, Slaveiko Neytchev, Slavka Tzanova, Dynamic Compensation of the Offset of an Integrated Hall Sensor with an Instrumentation Amplifier, 6th IMAPS International Symposium for Design and Technology of Electronic Modules, SIITME 2000, Bucharest, 21 -24 September, 2000, pp. 119-123

[4] C. Muller-Schwanneke, F. Jost, K. Marx, S. Lindenkreuz, K. von Klitzing, *Offset reduction in silicon Hall sensors*, Sensors and Actuators 81 (2000), Elsevier, pp. 18-22.

[5] R.G. Mani, K. von Klitzing, F. Jost, K. Marx, S. Lindenkreuz, H.P. Trah, Method for simultaneously reducing the misalignment offset and separating the Hall voltage from the off-diagonal piezoresistive voltage in Hall effect and piezoresistive devices based on silicon, Appl. Phys. Lett. 67 1994 2223.

[6] Ed Ramsden, *Hall Effect Sensors Theory Application*, Advanstar Communications, Cleveland, Ohio, 2001.

[7] Melexis Microelectronic Integrated Circuits, Datasheet, Programmable Linear Hall Effect Sensor MLX90251.