A 900 MHz Self-Tunable Narrowband Low-Noise Amplifier

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Abstract – **One design approach, which relate to self-tuning Low-Noise Amplifier (LNA) is considered in this paper. Phase control loop is introduced with aim to force filter central frequency to be equal to the input signal frequency. This is achieved by adjusting the amplifier resonant constituents. Thanks to that, the LNA is robust to parameter perturbations in the full tuning range and has constant maximum gain at central frequency. The 0.25 μm SiGe BiCMOS technology was used for design and verification of the LNA. The LNA has 20 dB gain, quality factor *Q* = 36 and central frequency from 880 up to 950 MHz. Simulation results indicate that the total noise is 1.16 μVrms, and –1 dB compression point is at 72.5 mV.**

Keywords – **Low-noise amplifier, Tunable, Phase Control Loop, Resonant circuit.**

I. Introduction

An inherent problem in implementing analog circuits is that the values of manufactured analog circuit components often differ from the design specifications because of process parameters, supply voltage, and temperature (PVT) variations. Due to these perturbations, the practically obtained results are not optimal. For instance, even a 1% discrepancy from the central frequency is unacceptable to fulfill frequency accuracy requirements in intermediate frequency (IF) filters, which are commonly used in receivers. Other solutions to compensate variations of frequency characteristics due to PVT variations are based on utilization of tunable filters, master-slave filter tuning schemes and self-tuning filters [1-3, 7]. The latter approach, as more challenging one, is proposed in this paper.

Tunable selective amplifiers can be realized by using digitally controlled binary-weighted capacitor array, or current mirror array [2]. The switching scheme is based on successive approximation algorithm. However, the frequency accuracy with digital tuning is constrained by the number of tuning (not > 5) bits used. This is done in order to avoid too much overhead in chip area and to minimize the parasitic effects of switch resistances, resulting in 5–10% frequency mismatch [2].

Analog filters and selective amplifier are also adjusted by master–slave tuning schemes [3, 7]. The most commonly used master-circuit is voltage-controlled oscillator (VCO), whereas a slave filter is built with identical integrators. However, there are some difficulties in matching filter characteristics with characteristics of the master VCO [1]. Superior approach is to use voltage-controlled filter as a master, what results in better matching between master and slave filters.

Each selective LNA at characteristic frequencies (cut-off, central frequency etc.) has defined phase shifts values. By comparing the phases of input and output signals, it is possible to detect the mismatch of filter characteristics. In order to obtain the desired phase transfer function, self-tuning filters use the estimated phase error as correction factor. In our proposal, to accomplish phase error correction we use a phase control loop, similar to one used in tuning oscillators with phase locked loop (PLL), or delay lines with delay locked loop (DLL) [4, 5].

Here we present a LNA architecture, which belongs to a class of self-tuning circuits. Two benefits arise from the proposed solution: (i) the LNA is always tuned to input signal frequency, even in a presence of huge parameter perturbations, and (ii), the LNA can be used as a selective amplifier in wide range of input signal frequencies.

The paper is organized as follows. Section II concentrates on realization of the tunable LNA. The structure of self-tuning LNA with phase control loop is defined and described in the Section III. Simulation results are presented in Section IV and self-tuning LNA application in Section V. Finally, Section VI contains some concluding remarks.

II. A Tunable Narrowband Low-Noise Amplifier

The LNA schematic, used in this paper, is based on one of the most popular topologies, known as inductively degenerated common source LNA [8]. The simplified circuit given in Fig. 1 (without bias and matching circuits) is composed of two MOS transistors, M_1 and M_2, LNA amplifier scheme. MOS transistor M_1, operates as common-source. The inductor L_{pr} is connected to a DC biasing node. The Miller effect for LNA circuit is very important. This effect strongly limits its frequency characteristics and provides poor reverse isolation. A cascode transistor M_2 operates in common-gate mode. It significantly decreases the Miller effect. By using two active elements, M_1 and M_2, high LNA gain is obtained.

The output load is implemented as resonant circuit consisting of L_1, C_1 and MVaricap. The voltage drop over the load is lower than the drop over a resistive load of the same impedance. This solution provides correct circuit operation at lower power supply voltage level (V_{dd} = 2.7 V), and has lower power dissipation.

MVaricap element corresponds to voltage controlled capacitor. In IHP BiCMOS technology, it is implemented as modified PMOS transistor [6]. By controlling polarization voltage of a N-well the capacitance between gate and channel of PMOS transistor varies. The value of a control voltage,

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V_{ctrl}, determines a capacitance of MVaricap element, so the resonant frequency, f_r, is given as

$$f_r = \frac{1}{2\pi\sqrt{L_1(C_1 + C_{\mathrm{MVaricap}})}} \qquad (1)$$

The dynamic impedance of a resonant circuits, at f_r, is very high so that the LNA has very high gain, too.

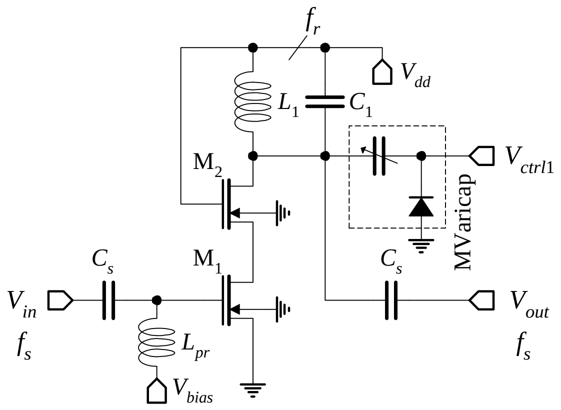

Fig. 1. Low-noise amplifier scheme

Elements of resonant circuit a selected in such way to obtain high quality factor, Q, and indirectly narrow LNA bandwidth, BW, so that

$$BW = \frac{f_r}{Q} \qquad (2)$$

In general, when BW is narrow LNA gain is high, receiver selectivity is good, attenuation of symmetrical signals in heterodyne receiver is high, and noise level is low. LNAs' amplitude and phase characteristics are obtained by simulation. By varying the control voltage, V_{ctrl}, within a range from 1.5 up to 2.7 V the LNA resonant frequency lies in the range from 880 up to 950 MHz, and maximal gain A = 20 dB. For Q = 36, BW = 25 MHz is obtained.

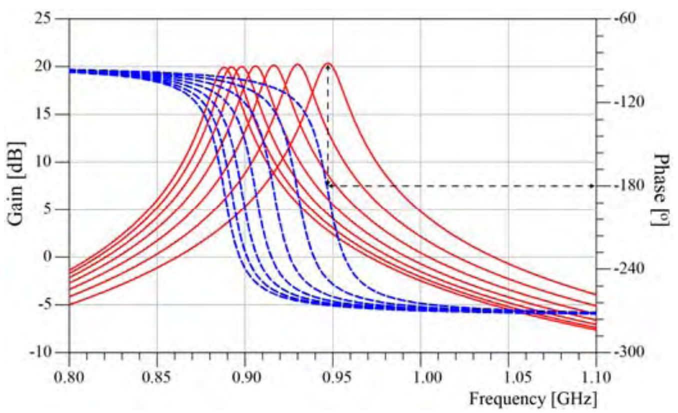

Fig. 2. Gain magnitude and phase characteristics

According to Fig. 2, and having in mind that the phase shift is defined as:

$$\theta(f_s) = -180 - \mathrm{atan}\left(2Q\frac{f_s - f_r}{f_r}\right) \qquad (3)$$

maximal gain, at resonant frequency, is obtained for phase shift of –180°.

III. Self-tuning LNA architecture

The concept of the self-tuning LNA is based on phase control strategy. The phase shift between input and output signals is used to generate control voltage, V_{ctrl}. The control voltage determines resonant frequency, i.e. indirectly the LNA phase characteristic. When the filter phase shift is –180°, then f_r is tuned to the frequency of the input signal f_s.

The basic idea of phase control is similar to one that we meet in DLL circuits [4, 5], with one exception: Instead of pulse delay control, as it is in DLL circuits, we control the phase shift of the output signal. Block diagram of the proposed circuit is given in Fig. 3. The LNA, introduced in Sec. 2, represents a building block of a self-tuning LNA architecture (see Fig. 3).

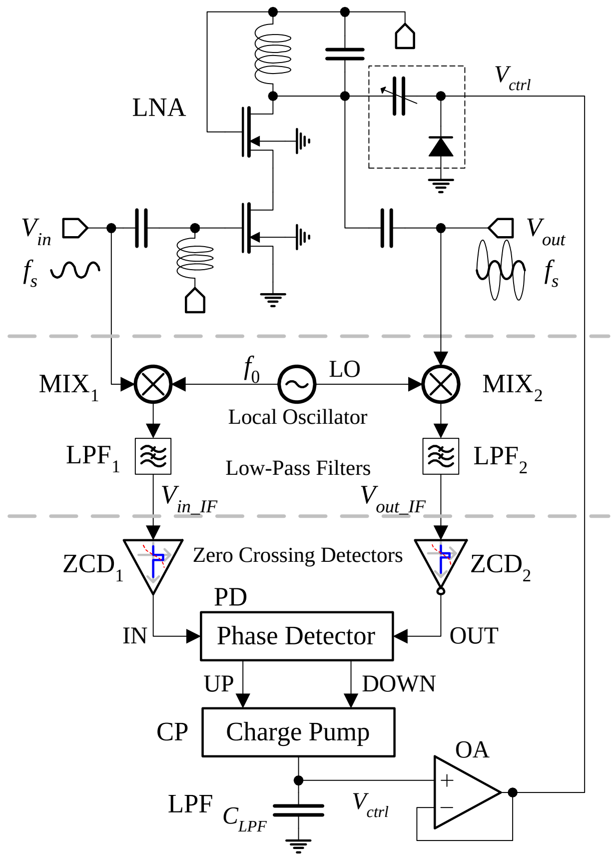

Fig. 3. Block diagram of self-tuning LNA architecture.

Correct operation of a phase detector is necessary to provide for accurate phase comparison. This is difficult to realize at high RF/MW frequency. Therefore frequency down conversion of signals V_{in} and V_{out} is performed by using two mixers, MIX_1 and MIX_2, local oscillator, LO, as generator of frequency f_0, and two low-pass filters, LPF_1 and LPF_2. This part of the circuits is given in Fig. 4. At the outputs of frequency down-converter two signals, V_{in_IF} and V_{out_IF}, are generated, but with lower frequency, $f_0 - f_s$, in respect to the frequency of RF signals, V_{in} and V_{out}.

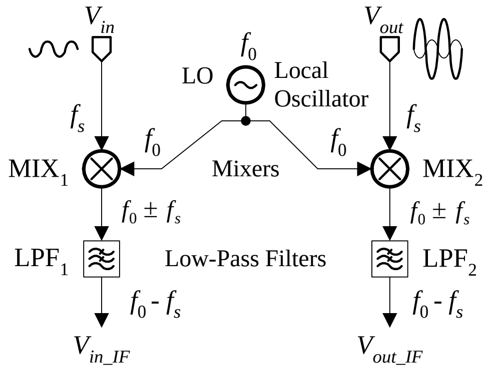

Fig. 4. Frequency down-conversion block

In order to estimate the phase shift between V_{out} and V_{in}, signals V_{out} and V_{in} amplified first, and after that they are shaped to rectangular forms. This is achieved by using two zero crossing detectors, ZCD1 and ZCD2.

Phase comparison of the input V_{in} and output V_{out} signals is performed by a phase detector (PD), which generates UP and DOWN signals. DOWN signal is on when the V_{out} phase leads in respect to the V_{in} phase, while in the opposite, UP signal is active. Time durations of UP and DOWN signals are proportional to the phase shift. UP and DOWN signals control the operation of a charge pump (CP). CP charges and discharges the load capacitor C_{LPF} providing V_{ctrl} that is used as control voltage for the LNA resonant frequency. In stable-state the phase shift between V_{out} and V_{in} signals is -180^o.

Unity gain operation amplifier is used as buffer stage, primarily to decouple the influence of C_{LPF} to MVaricap capacitance, i.e. to the resonant frequency.

ZCD is implemented by a circuit presented in Fig. 5. It is composed of CMOS inverter stages, denoted as I_1 to I_5. The first stage, I_1, acts as a linear amplifier. Since its input is capacitive coupled with the analog signal obtained from the LNA, it eliminates the DC offset. The other stages, I_2, I_3, I_4 and I_5, operate as digital inverters.

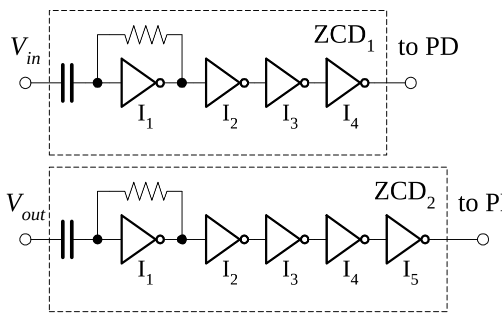

Fig. 5. Zero crossing detector

In systems with phase control loop (PLL and DLL) during stable state the phase difference between input and output signals is zero. The proposed LNA, in ideal case, involves phase shift of -180^o, therefore within the phase feedback loop is necessary to involve an additional phase shift of -180^o so that total phase shift be -360^o. The additional phase shift is obtained at the output of ZCD$_2$, by involving one inverter more, i.e. I_5.

More details about the structures a principles of operation of phase detector and charge pump circuits are given in [5, 7].

IV. Simulation Results

The proposed solution, which relates to design of self-tuning LNA with phase loop control, is verified by Spice simulation. The IHP design kit for 0.25 μm SiGe BiCMOS technology was used [6]. The supply voltage V_{dd} was chosen to be 2.7 V. AC characteristics of LNA, shown in Table I, were simulated first.

TABLE I
LNA CHARACTERISTICS

Gain	20 dB
Resonant frequency range	880 – 950 MHz
Bandwidth	25 MHz
Quality factor	36
Total noise	1.16 μVrms
–1 dB compression point	72.5 mV

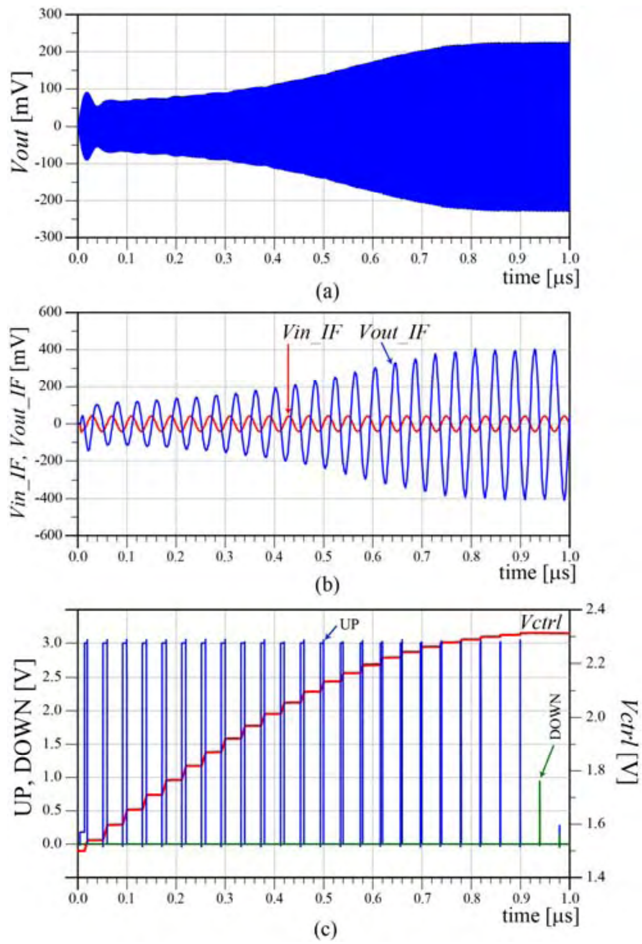

Fig. 6. Time response of the LNA with phase control loop: (a) V_{out} (b) V_{in_IF} and V_{out_IF} and (c) UP, DOWN and V_{ctrl}.

Our design goal was to realize selective LNA whose central frequency can be tuned. During the tuning process the LNA gain and bandwidth should be keep approximately constant. The tuning process, in our design, was performed by varying the capacitance MVaricap, what was achieved by adjusting a DC biasing point. Consequently, the resonant f_r frequency was subject to change.

Fig. 6 shows time responses of the self-tuning LNA with phase control loop. Settling time of the LNA output signal V_{out} is presented in Fig. 6(a). The phase control loop changes the referent resonant frequency of resonant circuits until a condition $f_r = f_s$ is fulfilled. At resonant frequency the LNA has maximal gain.

During this input signal of frequency f_s = 915 MHz and local oscillator with frequency f_0 = 940 MHz were used. Waveforms of the down-converted input V_{in_IF} and output V_{out_IF} signals that are used for driving the self-tuning LNA are presented in Fig. 6(b).

UP and DOWN control signals, obtained at the outputs of PD, as well as V_{ctrl}, are given in Fig. 6(c). The steady-state state is reached, i.e. the phase loop is locked, at the moment when: i) the signals V_{in} and V_{out} are of opposite phases, ii) UP and DOWN signals disappear, and iii) the control voltage V_{ctrl} has a constant value. The settling time of a system is approximately 900 ns.

V. Self-tuning LNA application

The application of LNA is given in Fig. 7. The structure consists of two LNAs, master and slave. The master LNA is excited by the referent frequency source f_s and it generates control voltage, V_{ctrl}. The slave LNA is of identical structure as the master. It is driven with the same control voltage V_{ctrl}, generated by the master LNA. The slave is used for amplification and filtering of the input signal.

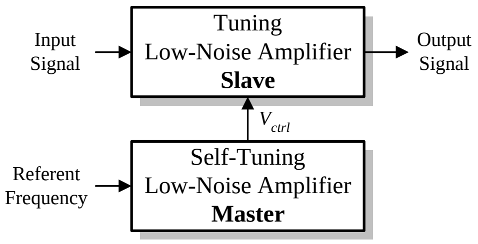

Fig. 7. Typical application for self-tuning band-pass filter

VI. Conclusion

In this paper we present architecture of self-tuning LNA, suitable for VLSI implementation. The central frequency is tuned by adjusting resonant frequency. The self-tuning LNA is operative in a defined frequency range (from 880 up to 950 MHz), and is characterized with relatively high quality factor Q, and high gain (20 dB), what makes this architecture suitable for realization of narrow-band amplifiers implemented in heterodyne receivers.

The phase control loop forces the filter central frequency to be equal to the input signal frequency. This is performed by changing MVaricap capacitance with control voltage, which is proportional to the integral of a phase error between filter input and output signals. The structure of a phase control loop is similar to standard phase/delay locked loop circuits [4, 5]. The proposed architecture (900 ns) provides short overall system settling time.

The IHP 0.25 μm SiGe BiCMOS technology was used during design and verification of the LNA. Simulation results show that the central frequency of LNA can be within the range from 880 up to 950 MHz. The LNA is designed as amplifier with 20 dB gain at central frequency, and with quality factor Q = 36. In addition, simulation results indicate that the total in-band noise is 1.16 μVrms and –1 dB compression point is at 72.5 mV.

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