Analysis and Design of Instrumentation Amplifiers

Ivailo Pandiev[1]

Abstract – **The paper presents the structure and the principle of operation of the basic instrumentation amplifier (in-amp) circuit employing three voltage-feedback operational amplifiers (VFOAs). Based on the analysis of the principle of operation are obtained equations for the transfer functions and formulas for the most important static and dynamic parameters. Moreover, using the obtained formulas is developed a design procedure and recommendations for simulation modeling, using standard and statistical analyses. The effectiveness of the proposed procedure is shown by simulation modeling of sample circuits of in-amps.**

Keywords – **Analogue circuits, In-Amps, Programmable gain in-amp, VFOA, Design procedure, Analogue simulation.**

I. INTRODUCTION

The instrumentation amplifiers (in-amps) are essential building blocks of data acquisition systems and are used to extract a weak signal from a noisy environment [1-3]. In the last ten years have been created many monolithic two- op amps and three- op amps in-amps [4-6]. Since for the monolithic in-amps the active and the passive components are implemented within the same semiconductor substrate, they can be closely matched. This will ensure that the amplifiers provide a high *CMRR*. In addition, these components will stay matched over temperature, ensuring good performance over a wide temperature range. In comparison with the monolithic in-amps, offered by the manufacturers of analogue ICs, the in-amps with discrete passive components propose design flexibility at low cost and can sometimes provide performance unattainable with monolithic amplifiers, such as high bandwidth.

The analysis of existing literature showed a wide variety of books and technical documents [1, 7-13], which discuss various aspects of the analysis and design of the in-amps. In [1] and [8-13] the attention of the authors is focused primarily on the principles of operation of the basic circuits of in-amps, as well as some recommendations for selecting the values of the feedback resistors are given. In [7] the authors presented a procedure for designing in-amps realized on the basis of the classic three- op amp circuit. Moreover, the procedure does not include recommendations for calculating the output offset voltage, as well as its temperature drift, frequency bandwidth and equivalent output noise voltage. Also in [7] are not defined recommendations for getting values of the feedback resistors to obtain an optimum value of the *CMRR*.

In this paper on the basis of theoretical analysis of the three- op amps in-amps with discrete passive components a new systematic design procedure is proposed.

[1]Ivailo Pandiev is with the Faculty of Electronics at Technical University of Sofia, 8 Kl. Ohridski Blvd, Sofia 1000, Bulgaria, E-mail: ipandiev@tu-sofia.bg.

II. THEORETICAL ANALYSIS OF THE THREE- OP AMPS IN-AMPS

An object of study is the circuit of the three- op amp in-amp, given on Fig. 1. The input section consists of two op amps with negative feedback through the resistors R_2, R_3 and R_{GAIN}. It has a symmetrical input and output. The output section of the circuit is a differential amplifier with a differential input U_{AD} and a single-ended output U_o with respect to a reference terminal *REF*.

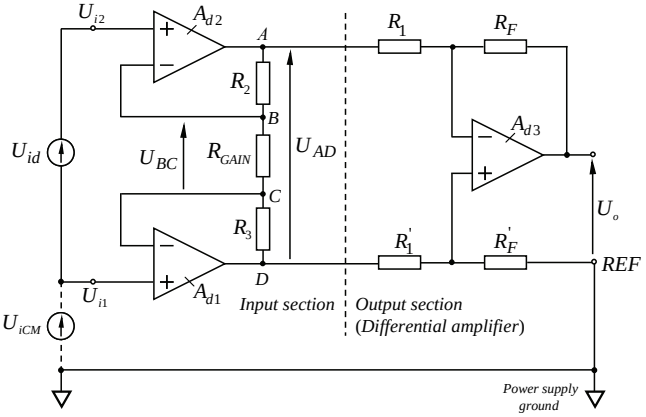

Fig. 1. A structure of the three- op amps in-amp circuit

At condition, that the op amps are ideal active elements and $\frac{R_F}{R_1} = \frac{R'_F}{R'_1}$ for the differential voltage gain is obtained

$$A_U = \frac{U_o}{U_{id}} = A_{U1}A_{U2} = \left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1}, \qquad (1)$$

where $A_{U1} = \frac{U_{AD}}{U_{id}} = 1 + \frac{R_2 + R_3}{R_{GAIN}}$ is the differential gain of the input section and $A_{U2} = \frac{U_o}{U_{AD}} = \frac{R_F}{R_1}$ is the differential gain of the output section.

From equation (1) it can be seen, that the necessary voltage gain for differential signals can be varied by changing the value of the resistor R_{GAIN}, without affecting the symmetry of the circuit. If $R_{GAIN} = \infty$ the input section operates as a voltage follower and the differential voltage gain of the circuit is determined only by the gain of the output section.

At condition, that the op amps are real active elements ($A_d \neq \infty$) at high frequencies the open-loop voltage gain is a complex quantity, which in the most cases can be approximated with a first-order transfer function, according to the following equation

$$\dot{A}_d = \frac{A_{d0}}{1 + j(f / f_p)}, \quad (2)$$

where A_{d0} is the low-frequency open-loop voltage gain and f_p is the dominant pole of the op amps.

Then the total complex voltage gain of the in-amp is obtained as a second-order transfer function, containing two real poles. Thus the pole frequencies at R_2=R_3=R are

$$f'_{p1} = f_{p1(2)}(1 + \beta_1 A_{d0,1(2)}) \text{ and} \quad (3a)$$

$$f'_{p2} = f_{p3}(1 + \beta_2 A_{d0,3}), \quad (3b)$$

where $A_{d0,1(2)}$ and $A_{d0,3}$ are the low-frequency open-loop gains of the input and output sections, $f_{p1(2)}$ and f_{p3} are the dominant pole frequencies of the op amps and $\beta_1 = \frac{R_{GAIN}/2}{R + R_{GAIN}/2}$ and $\beta_2 = R_1/(R_1 + R_F)$ are the feedback coefficients of the input and output section, respectively.

In the cases when $A_{U1} > A_{U2}$ the pole frequency of the input section determines the cutoff frequency of the in-amp at high frequencies, i.e. the cutoff frequency f_h corresponds to value of the pole frequency f'_{p1}.

Since each part of the input section on Fig. 1 is a non-inverting amplifier, the input resistance of the in-amp is high and is equal to

$$R_{iA} = 2\{2r_{iCM} \parallel [r_{id}(1 + \beta_1 A_{d0})]\}, \quad (4a)$$

where r_{iCM} is the common-mode input resistance, r_{id} is the differential-mode input resistance and A_{d0} is the open-loop voltage gain of the input op amps.

The output resistance is small and is determined by

$$R_{oA} \approx \frac{r_o}{A_{d0,3}}\left(1 + \frac{R_F}{R_N}\right), \quad (4b)$$

where r_o is the output resistance of the output op amp.

If to the both inputs of the in-amp common-mode voltage ($U_{i1} = U_{i2} = U_{iCM}$) is applied, then $U_B = U_C = U_{iCM}$ and $U_A = U_D = U_{iCM}$. Therefore, the common-mode gain of the input section is equal to one.

Then mathematically, the total common-mode rejection of the in-amp is

$$CMRR = A_{U1} CMRR_3, \quad (5)$$

where $CMRR_3 = CMRR_{\delta_R} \parallel CMRR_{A_3}$, $CMRR_{A_3}$ is the common-mode rejection of the output amp and $CMRR_{\delta_R} = (1 + R_F / R_1)/4\delta_R$ (δ_R is the tolerance of the resistors R_1, R_F, R'_1 and R'_F).

The total output offset voltage of the in-amp on Fig. 1, caused by the simultaneous action of the input offset voltages $U_{io1(2)}$ and currents $I_{io1(2)}$ of the op amps is

$$U_{o,err} = (U_{io1} - U_{io2})\left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1} + U_{io3}\left(1 + \frac{R_F}{R_1}\right) - I_{io3}R_F$$

In the worst case $U_{io1} = -U_{io2}$, then the value of the output offset voltage is

$$U_{o,err(\max)} = 2U_{io1}\left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1} + U_{io3}\left(1 + \frac{R_F}{R_1}\right) - I_{io3}R_F. \quad (6)$$

During the implementation of the input section with dual op amp it is possible the output offset, determined by the input offset voltages, to be compensated. The monolithic dual op amp has the advantage, that its components are implemented with the same microelectronic technology and have equal temperature drifts. However, obtaining the same electrical parameters of the two amplifiers is largely accidental. For the worst case the output offset voltage $\Delta U_{o,err}$, produced by the temperature drift of the $U_{io1(2)}$ and $I_{io1(2)}$, is

$$\Delta U_{o,err} = 2\Delta U_{io1}\left(1 + \frac{R_2 + R_3}{R_{GAIN}}\right)\frac{R_F}{R_1} + \Delta U_{io3}\left(1 + \frac{R_F}{R_1}\right) - \Delta I_{io3}R_F, \quad (7)$$

where $\Delta U_{io} = \alpha_{U_{io}}\Delta T$ and $\Delta I_{io} = \alpha_{I_{io}}\Delta T$ ($\alpha_{U_{io}}$ and $\alpha_{I_{io}}$ are the average temperature coefficients of the input offset voltage and current, respectively).

III. DESIGN PROCEDURE

The above analytical formulas, as a result of the theoretical analysis, are the base of the design procedure for the three-op amp in-amps. The schematic design for the circuit on Fig. 1 is based on the following sequence:

1. *Technical specification.* The circuit elements are calculated using pre-defined: amplitude of the differential-mode input voltage U_{id} or amplitude of the input differential voltage source e_G with internal resistance R_G; amplitude of the input common-mode voltage U_{iCM}; input resistance R_{iA}; amplitude of the output voltage U_{R_L} and load resistance R_L; output resistance R_{oA}; cutoff frequency f_h at maximum acceptable attenuation coefficient M_h; relative error ε_{io} [%] defined by the input offset current and voltage, as well as their

temperature drift $\varepsilon_{\Delta io}$ [%] within temperature range ΔT; minimum value of a signal-to-noise ratio SN [dB].

2. *An electronic circuit is selected.* An object of an analysis and design is the in-amp circuit shown on Fig. 1. If assume that $R_2 = R_3 = R$ and $R_1 = R_1^{'} = R_F = R_F^{'}$, then $A_{U2} = 1$ and $A_U = A_{U1}$. Based on the formulas (1) and (5) for the differential gain and common-mode rejection are received

$$A_U = \frac{U_{om}}{U_{id}} = 1 + \frac{2R}{R_{GAIN}} \text{ and } CMRR = \left(1 + \frac{2R}{R_{GAIN}}\right)\frac{1}{2\delta_R}.$$

The typical values for the differential gain A_U are in the range $1 \dots 10^3$. In the case that with the selected op amp can not be achieved the desired differential gain A_U, but it gets the desired value of the CMRR for the designed in-amp consequently an inverting or a non-inverting amplifier circuit, employing VFOA has to be connected [2].

3. *The op amps are selected.* For the implementation of the input section usually is selected dual precision op amp (for example OP2177 or AD8698) with high common-mode rejection ($\geq 100dB$), small input bias currents ($< 1nA$), and small input offset voltage ($< 1mV$). The output op amp is a single precision amplifier (for example OP1177 or OP177), that provides the maximum output voltage at a given load. Usually for the precision op amps the maximum output current does not exceed several mA and they no have short-circuit current protection. In addition to the pin marked with REF, can be applied an external voltage V_{REF} from a reference voltage source. The V_{REF} define the signal ground of the in-amp at single power supply. The op amps of the circuit are selected according to the following conditions:

− Common-mode rejection: $CMRR_{A_{1(2,3)}} \geq 10 \times CMRR$;

− Maximum output voltage for the op amps of the input section: $U_{om,A_{1(2)}} \geq U_{om} + U_{iCM}$ ($U_{om,A_{1(2)}}$ is the maximum output voltage of the input op amps);

− Maximum output voltage of the output op amp: $U_{om,A_3} \geq U_{om} + V_{REF}$ for $V_{REF} \neq 0$ (U_{om,A_3} is the maximum output voltage of the output op amp);

− The power supply voltage $\pm V_{CC}$ is selected higher than maximum output voltages $U_{om,A_{1(2)}}$ and U_{om,A_3}, as saving the condition $V_{CC\min} < V_{CC} < V_{CC\max}$;

− Maximum output current $I_{o\max,A_3} > I_{om}$, where $I_{om} = U_{om} / R_L$ (for $V_{REF} \neq 0$ is found $I_{om} = (U_{om} + V_{REF}) / R_L$);

− Small-signal bandwidth of the input op amps: $f_{pA_{U01(2)}}^{'} \geq f_h^{'}$, where $f_h^{'} = f_h / \sqrt{M_h^2 - 1}$ and $f_{pA_{U01(2)}}^{'}$ is a cut-off frequency of the closed-loop gain $|\dot{A}_U| = A_U(f)$;

− Small-signal bandwidth of the output op amp: $B_{1,A_3} \geq f_h^{'}$, where $f_h^{'} = f_h / \sqrt{M_h^2 - 1}$ and B_{1,A_3} is the unity gain bandwidth;

− Slew rate is selected $SR_{A_{1(2,3)}} > 2\pi f_h^{'} U_{om}$.

4. *The values of the feedback resistors R_2 and R_3 are selected*: Select $R_2 = R_3 = R$. These resistors should be larger than the minimum value $R_{2\min} = U_{om,A_{1(2)}} / I_{o\max,A_{1(2)}}$. Otherwise, it can be overload the output stages of the input op amps. On the other hand, the resistance R_2 have not be greater than the maximum value $R_{2\max}$, for precision op amps the resistance have not be higher than $1 \dots 2M\Omega$. For larger values of R_2 it increases the influence of the U_{io}, I_{io} and noise.

5. *The value of the gain resistor R_{GAIN} is calculated*:

$$R_{GAIN} = 2R / (A_U - 1).$$

For the resistors R_2, R_3 и R_{GAIN} are selected standard values, usually with a tolerance of $\pm 1\%$ or less.

6. *The values of the feedback resistors R_1, $R_1^{'}$, R_F and $R_F^{'}$ are selected*: Select $R_1 = R_1^{'} = R_F = R_F^{'}$ ($A_{U2} = 1$).These resistors should be larger than the minimum value $R_{F\min} = U_{om,A_3} / I_{o\max,A_3}$. Otherwise, it can be overloaded the output stage of the output op amp. On the other hand, the resistances have not be greater than $1 \dots 2M\Omega$.

7. *The necessary value of the tolerance δ_R of the resistors R_1, $R_1^{'}$, R_F and $R_F^{'}$ are calculated*:

$$\delta_R \leq \frac{A_U}{2 \times CMRR}.100\%.$$

8. *The input and output resistance is calculated using Eq. (4a) and (4b), respectively*. The obtained values for the input and output resistance is compared with the values given in *step 1* of the procedure.

9. *The output offset voltage of the circuit is calculated.* First the output offset voltage for room temperature (usually in data-sheets the input offset voltage and current of the op amp is defined at $25°C$) is calculated according to Eq. (6). Then the relative error $\varepsilon_{io} = (U_{o,err} / U_{R_L})100\%$ is compared with the value given in *step* 1.

10. *The output offset voltage drift is calculated.* First the output offset voltage drift is calculated by Eq. (7) for the given temperature range ΔT. Then the relative error $\varepsilon_{\Delta io} = (\Delta U_{o,err} / U_{R_L})100\%$, is compared with value the given in *step* 1. If the results for ε_{io} and $\varepsilon_{\Delta io}$ do not satisfy the specification it can be chosen more precision op amps or to make new calculations for the resistances with lower values.

11. *The signal-to-noise ratio (SN) is calculated*. First the resulting noise density at the amplifier's output is calculated:

$$\bar{S}_{U,out} = \sqrt{\sum_i S_{U_i}^2} \text{ for } i = 1, 2, \dots,$$

where S_{U_i} is the individual noise components.

Then $SN = \frac{U_{o,eff}}{U_{oN}} = \frac{U_{o,eff}}{\bar{S}_{U,out}\sqrt{B_{eq}}}$, where $B_{eq} = 1{,}57\, f_h^{'}$ is the bandwidth of the circuit multiplied by the correction factor of $\pi/2 \approx 1{,}57$ and $U_{o,eff}$ is the output effective value.

12. *Verification check of the designed in-amp in DC and AC domain by using Cadence OrCAD®.*

IV. Simulation Testing and Analyses

To verify the theoretical analysis and the proposed procedure a digitally programmable gain in-amp (PGiA) (Fig. 2) was implemented with the following pre-defined parameters: $U_{id} = 0...\pm 10mV$, $\pm 20mV$, $\pm 40mV$ and $\pm 80mV$ at $R_G = 5k\Omega$; $R_{iA} \geq 10M\Omega$; $A_U = 250$, 125, 62,5 and 31,25 at $R_L = 2k\Omega$; $CMRR \geq 90dB$; $R_{oA} \leq 1\Omega$; $f_h = 100Hz$ at $M_h = 3dB$; $\varepsilon_{io} < 0{,}5\%$, $\varepsilon_{\Delta io} < 0{,}2\%$ (within temperature range $\Delta T = 40°C$); $SN_{\min} > 80dB$.

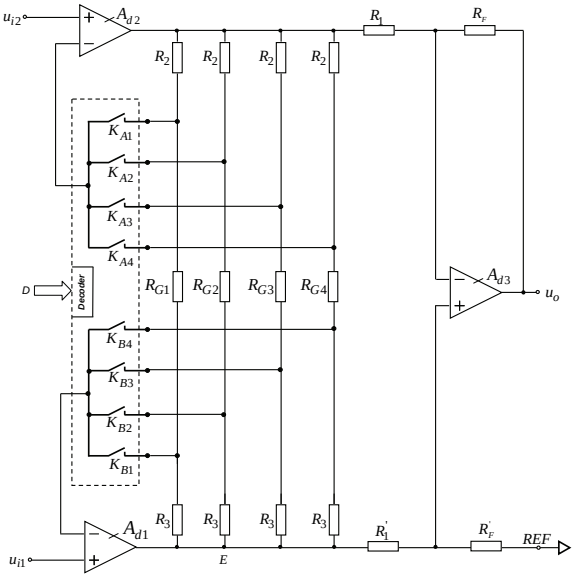

Fig. 2. A structure of the designed PGiA circuit

The circuit is designed using VFOA OP1177 and OP2177 (from Analog Dev.), biased with $\pm 5V$ supplies. The verifycation check of the circuit was performed within OrCAD PSpice, using corresponding PSpice-based macro-models. The models reflect typical values of the datasheet parameters for power supply voltages $\pm 15V$ and not capable of simulating some of the input parameters and the temperature effects.

The values of the calculated passive in-amp components are: $R_2 = R_3 = 10k\Omega \pm 1\%$, $R_{G1} = 80{,}6\Omega \pm 1\%$ (at $A_{U1} = 250$), $R_{G2} = 162\Omega \pm 1\%$ (at $A_{U2} = 125$), $R_{G3} = 324\Omega \pm 1\%$ (at $A_{U3} = 62{,}5$), $R_{G4} = 665\Omega \pm 1\%$ (at $A_{U4} = 31{,}25$) and $R_1 = R_1^{'} = R_F = R_F^{'} = 10k\Omega$ with tolerances $\pm 0{,}1\%$. The controlling digital word D for the in-amp will provide gains of 31,25, 62,5, 125 and 250, through synchronous switching of the two groups of switches (K_{A1}-K_{A4}) and (K_{B1}-K_{B4}) with the decoder.

In Table 1 are presented the calculated parameters and the simulation results for the designed in-amp. The maximum error between calculated values of the electrical parameters and the simulation results is not higher than 5%. Moreover, an error of 5% is quite acceptable considering the tolerances of the technological parameters.

TABLE I
COMPARISON BETWEEN CALCULATED PARAMETERS AND SIMULATION RESULTS FOR THE DESIGNED IN-AMP.

Parameter	***Cal. results***	***Sim. results***
$U_{o,err}$	from 0,03m*V* to 1…7,5m*V*	from 0,032m*V* to 0,95…7,56m*V*
ε_{io}	from 0,001% to 0,04…0,3%	from 0,0012% to 0,038…0,3%
$\Delta U_{o,err}$	from 0,014m*V* to 0,5…4m*V*	n/a
$\varepsilon_{\Delta io}$	from 0,0005% to 0,02…0,16%	n/a
U_{om}	2,5*V*	2,5*V*
f'_h at A_U = 250, 125, 62,5 and 31,25	5,68k*Hz*, 11,4k*Hz*, 22,7k*Hz*, 45,5k*Hz*	5,75k*Hz*, 11,5k*Hz*, 22,3k*Hz*, 45,6k*Hz*
R_{iA} / R_{oA}	$2.10^{12}\Omega$ / 0,03mΩ	$1{,}93.10^{12}\Omega$ / 0,03mΩ
CMRR	90*dB*	$96{,}38_{\min}$ … $98{,}26dB_{\max}$
$\bar{S}_{U,out}$ at R_{G1}=80,6Ω	2,85$\mu V/Hz^{1/2}$	2,91$\mu V/Hz^{1/2}$
SN	93,9*dB*	93,7*dB*

V. Conclusion

A design procedure of three- op amp in-amp circuits has been presented. The efficiency of the procedure is demonstrated by design and verification of concrete electronic circuits using precision VFOAs OP1177 and OP2177. The created approach can be useful for design of various electronic devices, such as precision amps, PGiAs and high-speed video amps.

References

[1] Kitchin, C., L. Counts. *A Designer's Guide to Instrumentation Amplifiers*, 3rd Addition, Analog Dev., 2006.

[2] W. Jung, *Op Amp Applications Handbook*, Newnes, 2005.

[3] V. Tietze, Ch. Schenk. *Electronic circuits*. 2nd Edition. New York. Springer-Verlag, 2008.

[4] Instrumentation Amplifiers, Analog Dev., http://www.analog.com, last accessed February 20, 2013.

[5] Instrumentation Amplifiers, Texas I., http://www.ti.com, last accessed February 20, 2013.

[6] Instrumentation Amplifiers, Linear Tech., http://www.linear.com, last accessed February 20, 2013.

[7] V. Zlatarov *et al*. *The designer's guide to analog circuits and systems*. Tehnika, Sofia, 1993 (in Bulgarian).

[8] R. Mancini, *Op Amps for Everyone Design Guide* (Rev. B), Texas I., 2002.

[9] M. Seifart, *Analoge Schaltungen*. 6 Auflage. Verlag Technik Berlin, 2003 (in German).

[10] T. Kugelstadt, Getting the most out of your instrumentation amplifier design. Texas I., Analog Applications Journal, 2005.

[11] Instrumentation Amplifier. AN1298.2, Intersil, 2009.

[12] N. Albaugh, *The instrumentation amplifier handbook*, Cypress Semiconductor, 2012.

[13] J. Li, S. Pun, M. Vai, P. Mak, P. Mak, F. Wan. "Design of Current Mode Instrumentation Amplifier for Portable Biosignal Acquisition", BioCAS 2009, pp. 9-12, Beijing, 2009.