Start-Stop Ring Oscillators for GALS Designs

Goran Jovanović[1] and Mile Stojčev[1]

Abstract – **The tendency of integrating a whole digital signal processing or communication system in a single chip, referred as System-on-Chip (SoC) design, becomes nowadays pronounced. The main design challenges in realization of such complex VLSI IC systems deal with high-speed of operation, low-power of consumption, high flexibility, etc. Voltage controlled oscillators are broadly used, as basic building blocks, in this type of applications, mainly intended for controlling asynchronous data transfer between different macro-blocks within a SoC design. Even the fact that diverse structures exist for realization of voltage controlled oscillators, the ring configuration is very attractive due to wide tuning range it can achieve, its operation at low voltage, small silicon area, and possibility to integrate this oscillator in standard CMOS process. In this article we investigates performance of ring oscillators constructed from several different types of inverting gates (used as delay elements) available in library (in our case it is 130 nm SiGe IHP technology), in order to determine the operating frequency in terms of power supply voltage variations, temperature variations, and the number of delay stages in the ring oscillator structure. The proposed design solutions are suitable to be used as start-stop oscillators, mainly intended for reliable data transfer between macro-blocks within a SoC operating in different clock domains.**

Keywords –**Ring Oscillator, Start/stop oscillator, GALS design.**

I. INTRODUCTION

Voltage controlled oscillators (VCOs) are one of the commonly used building blocks for analog and mixed-signal circuits that we meet in communication and digital signal processing applications like phase- locked loops (PLLs), frequency synthesizers, clock and data recovery circuits, etc [1]. Generally, VCOs can be roughly categorized into the following two types [2]: i) tuned VCOs- harmonic oscillators such as Hartley-, Colpits-, Pierce-, Wien Bridge-, crystal-oscillators, etc. These oscillators consist of an amplifier to offer signal gain and a frequency feedback-selective network to feedback a selected frequency range to the input; and ii) non-linear VCOs- two different types of non-linear oscillators exist; j) relaxation oscillators- the output frequency is determined by the time spent in charge/discharge capacitors; and jj) ring oscillators (RO)- cascaded combination of delay stages connected in a close loop chain, and commonly used in the clock generation subsystem within a VLSI circuit.

Due to flexibility for on-chip integration CMOS based RO configuration becomes an attractive design solution having in mind the following advantages [1]: 1) it can be easily designed with the state-of-art CMOS and BiCMOS VLSI IC technology, i.e. small size of integration; 2) it can achieve its oscillations at low-voltage; 3) it can provide high frequency oscillations with dissipating relatively low power; 4) it can be electrically tuned; 5) it can provide easy control in wide tuning range; 6) it can provide multiphase outputs, i.e. generates a multiphase digital clock signals; and 7) no requirements for on-chip inductor for which realization large silicon area is needed. Compared to tuned VCOs some drawbacks of ROs include larger power consumption, higher phase noise, poorer frequency stability, and the limit of highest achievable frequency. Several types of ring VCOs have been reported in literature using different types of delay cells including multiple feedback loops, single ended delay cells, and dual-delay paths [3].

Here in focus of our interest are single ended ring VCOs because it is easy to integrate these structures in CMOS technology, give wide tuning range, and operates at low-voltage.

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II. RING VCO

A single ended inverter base ring VCO block diagram is shown in Fig. 1.

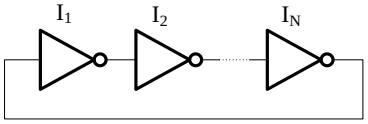

Fig. 1. Block diagram of single ended VCO

A ring oscillator consists of number of gain stages in a loop with the output of the last stage feed back to the input of the first. The ring must satisfy Barkhausen criteria according to which it should provide a phase shift of 2π and must have unity voltage gain to achieve oscillation. Each delay should provide phase shift of π/N, where N is the number of delay sages. The remaining π phase shift is provided by dc inversion. Single ended oscillator requires odd number of stages for dc inversion. Frequency of oscillation for N stage delay ring VCO is given by

$$f_0 = \frac{1}{2N\tau} \tag{1}$$

where τ is a propagation delay of each inverter stage.

From eq. (1) one may conclude that the number of inverter stages, N, used in the ring structure and the propagation delay, τ, of the delay stages limit the oscillation frequency f0 of the RO. The increase of oscillation frequency can be achieved in two ways: a) by reducing the propagation time delay τ of inverter stages; or b) by decreasing the number of stages N in the ring structure. The reduction of N is attractive not only for

the purpose of operational speed increment but also for power consumption reduction and saving in the silicon area for RO implementation in ICs. But in such design solutions the number of available multiphase outputs reduces with the decrease of N. From the other hand, the delay τ of each stage depends on the circuit structure and process parameters.

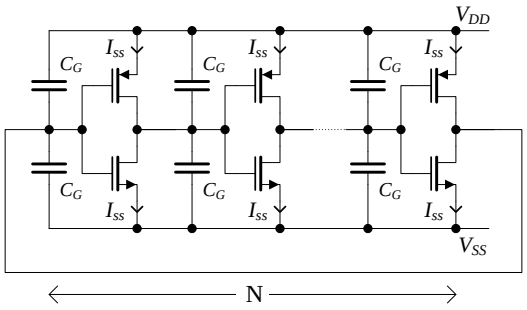

Fig. 2. Conventional voltage controlled ring oscillator

Let a conventional voltage controlled RO be given in Fig. 2. Assume that the gate to source parasitic capacitance of the NMOS and PMOS transistors are equal as is shown in Fig. 2. The difficulty in obtaining a value for the frequency arises when trying to determine τ, mainly due to nonlinearities and parasitic of the circuit. As is referred in [4] the delay per stage is defined as the change in the output voltage at the midpoint of the transition, V_{SW}, divided by the slew rate I_{SS}/C_G, resulting in a delay per stage of C_G*V_{SW} / I_{SS}. Using definition (1), the oscillation frequency is given by

$$f_0 = \frac{Iss}{2NV_{SW}C_G} \qquad (2)$$

For the given number of inverter stages, N, the oscillation frequency f_0 can be controlled by varying the current I_{SS}, or amplitude V_{SW} only, since C_G is usually fixed parameter. The smallest propagation delay time is determined by the structure of the inverter stage, process parameters and design technology, and can be controlled by incorporating additional voltage control delay (may be capacitive or resistive load) at the output of the inverter stage.

III. Structure of Inverter Stages

This paper extends our prior work [5] with additional analysis and results for six different library types of inverter stages and deals with details related to dependency of RO oscillating frequency in terms of voltage and temperature variations. As we have already mentioned single ended ring oscillators are realized with N inverter stages, where N is an odd number, Fig. 3. For synthesis of the inverter stage in our cell library, we have at disposal the following six different types of inverters: (a) basic inverter; (b) current starved with power switching; (c) current starved with output switching; (d) inverter with symmetric-load; (e) inverter based on NAND gate; and (f) inverter based on NOR gate. Designs presented in Fig. 4 (b), (c) and (d) are of current starved type for which the charging and discharging current is limited by a bias voltage. More details related to realization of these types of inverter stages can be found in Reference [6]. Designs presented in Fig. 4 (a), (e) and (f) correspond to classical (basic) inverter, NAND logical gate, and NOR logical gate, respectively.

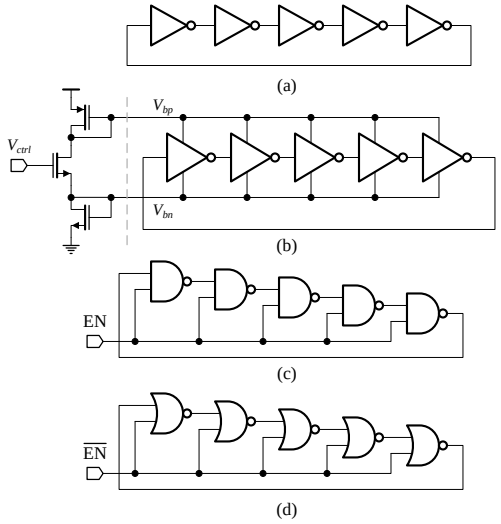

Fig. 3. Logical structures of single ended ring oscillators: (a) basic inverter; (b) current starved; (c) NAND gates; (d) NOR;

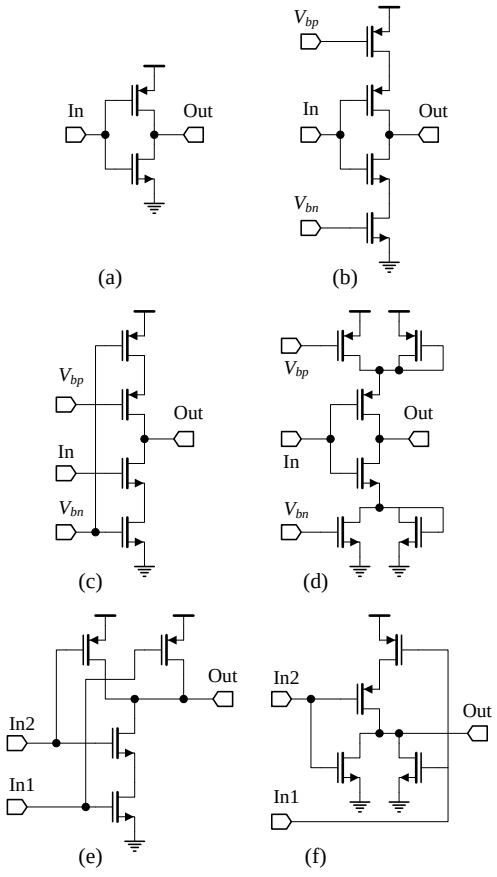

Fig. 4. Electrical schemes of delay elements: (a) basic inverter; (b) current starved with power switching; (c) current starved with output switching; (d) current starved with symmetrical load; (e) NAND gates; (f) NOR;

IV. Simulated Results

Our primary interest, in this paper, was to investigate the performance of all design solutions concerning the range of frequency regulation in terms of voltage and temperature variations (i.e., sensitivity to these variations), in order to choose the best design for a given application. The results obtained by simulation are presented in Fig. 5 and 6, respectively. For all ring structures the number of delay stages N=5.

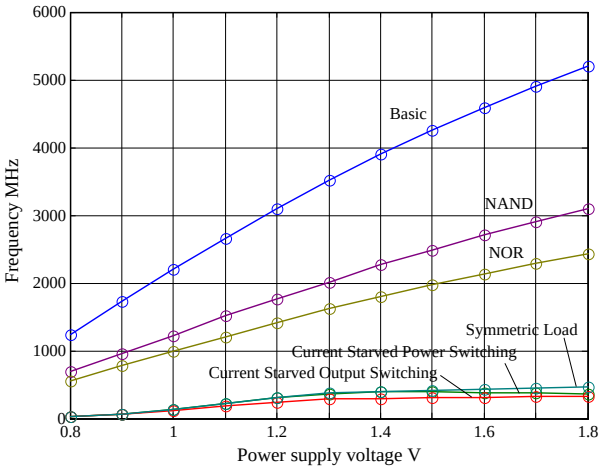

Fig. 5. Operating frequency in terms of power supply voltage

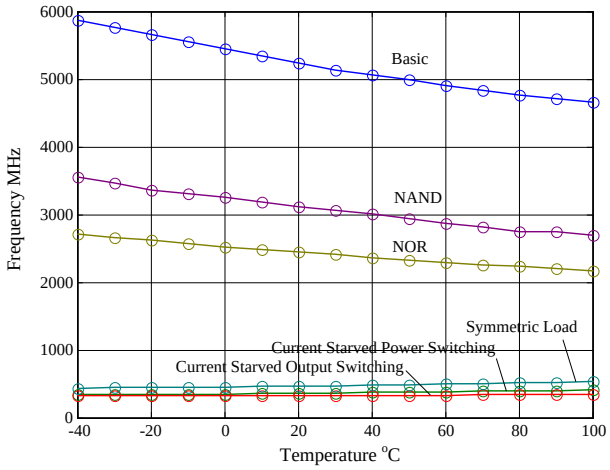

Fig. 6. Operating frequency in terms of temperature

By analyzing the simulation results presented in Fig. 5 and 6 we can conclude the following:

1. Having in mind that the basic (current starved output switching) delay stage involves minimal (maximal) time delay τ, by using this ring oscillator structure a highest (lowest) oscillator operating frequency can be achieved. The operating frequency (for working ambient temperature of 25°C) is within a range from 1.2 up to 5.2 GHz for highest (25-390 MHz for lowest) for power supply voltage variations from 0.8 up to 1.8 V, respectively. All other design solutions lie within these boundaries.

2. Similarly, the ring oscillator based on basic (current starved output switching) delay cells has highest (lowest) sensitivity to temperature variations. For temperature variations typical for the industrial range (from -40 up to 100°C) and for fixed power supply voltage of 1.8 V, the oscillating frequency is within a range from 5.9 down to 4.7 GHz for highest (335-405 MHz for lowest). The other designs of ring oscillators generate output frequencies within these limits.

In Table I the results which relate to the average ring oscillator sensitivities in terms of voltage and temperature variations are given. Again, the sensitivity of the basic inverter (current starved with output switching inverter) is highest (lowest) 4 MHz/mV (0.3 MHz/mV) for voltage variations, and –8 MHz/K (0.25 MHz/K) for temperature variations, respectively.

Table I
Average Sensitiveness of Ring Oscillator

Type	$\frac{df_0}{dV}\left[\frac{\text{MHz}}{\text{mV}}\right]$	$\frac{df_0}{dT}\left[\frac{\text{MHz}}{\text{K}}\right]$
basic inverter	4	–8
current starved with power switching	0.4	0.5
current starved with output switching	0.3	0.25
inverter with symmetric-load	0.5	0.8
NAND gate	2.2	–6
NOR gate	0.95	–2

V. Ring Oscillator for GALS Application

Contemporary SoC designs suffer from several problems, including: wire connection complexity, cross talk, data synchronization, multiple clock sources, etc. Here we will focus on multiple clock-sources issue. Within a SoC a unique and global clock source will limit the chip design performance and therefore each macro-block (IP core) cannot run at maximum speed because of the clock skew. To cope efficiently with this problem a Globally Asynchronous Locally Synchronous (GALS) designs are used.

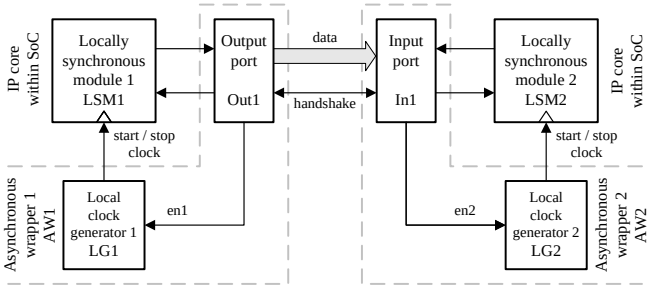

Fig. 7. Topology of pausable GALS

In a GALS design the communication between the synchronous IP cores (macro-blocks) occur asynchronously. Usually, a GALS system consists of a number of locally synchronous modules each surrounded with an asynchronous wrapper. Communication between synchronous blocks is

performed indirectly via asynchronous wrappers. Several GALS design styles have been proposed in literature such as pausable clocking scheme, asynchronous and loosely synchronous [7]. We are interested about pausable clocking scheme because it is the simplest one and based on usage a start-stop ring oscillator (see Fig. 7).

Data transfer between Locally Synchronous Modules LSM1 and LSM2 is performed during the following steps:

1. Initially we assume that both ports Out1 and In1 are empty, and local clock generators LG1 and LG2 are disabled.
2. When the Out1 is empty the enable signal en1 is activated and the start-stop local clock generator LG1 is activated.
3. After several clock pulses data from LSM1 is transferred to port Out1, the signal en2 is deactivated and LG1 stops its operation.
4. The handshake procedure for data transfer from port Out1 to port In1 is activated. As a consequence the enable signal en2 becomes active and the start-stop clock generator LG1 is activated.
5. After several clock pulses data from port In1 is accepted by LSM2, the signal en2 is disabled and LG2 stops its operation.

In a given design solution, both building blocks LG1 and LG2 are realized as start-stop single-ended three-stage ring oscillators (see Fig. 8).

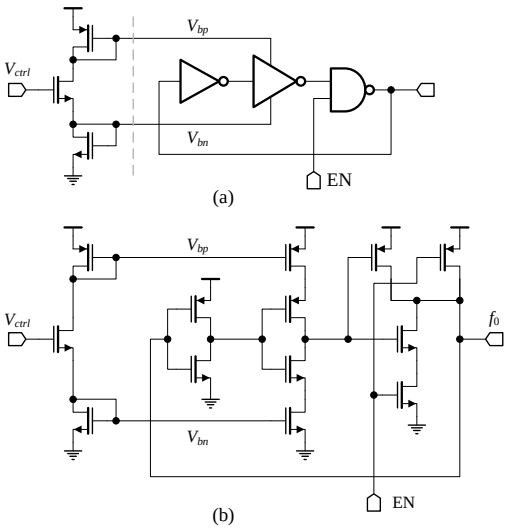

Fig. 8. Three stage single ended start/stop ring oscillator: (a) logical; (b) electrical scheme;

For a given ring oscillator, presented in Fig. 8, we obtain $\frac{df_0}{dV} = 1.1\left[\frac{\text{MHz}}{\text{mV}}\right]$ and $\frac{df_0}{dT} = 0.075\left[\frac{\text{MHz}}{\text{K}}\right]$.

The benefits of using start/stop ring oscillator in a given design are the following: (a) the structure of RO is simple, occupied silicon area is small; (b) RO always starts its operation with known phase what simplifies the realization of Out1/In1 handshake control logic; (c) most of the time RO is in inactive state (duty cycle < 1%), power consumption is low; (d) data transfer is high, RO oscillating frequency is 2 GHz.

VI. Conclusion

Many applications like frequency synthesizers, data clock recovery circuits for serial data communication, and start-stop oscillator as interface electronics in GALS designs (intended for parallel data transfer between macro-blocks within a SoC) reported ring structures. Ring oscillators have not only wide tuning voltage range but also have multiphase outputs which is an unique future of ring oscillators what make them attractive for realization of a control logic. The period of oscillation generally depends linearly upon the delay of each stage, which must be tuneable to obtain a controlled oscillator. In this paper, we investigate realization of five different types of five-stage single-ended ring oscillators based on usage of library available standard inverter gate stages for 130 nm SiGe IHP technology [8]. By conducting a comparative analysis of all candidate architectural designs our primary goal was to percept the dependence of oscillating frequency in terms of voltage and temperature variations. In a given case the characteristics of the proposed single-ended start-stop ring oscillator are highly attractive for its use in high-speed (2GHz) GALS interface within a SoC, and low-power consumption achieved thanks to low duty-cycle (<1%) operating principle of the ring oscillator.

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