Design and Realization of a Low Noise Power Converter

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Abstract – **In this paper the straightforward design of a low noise power converter is presented. The converter was built and tested through lab measurements. Design steps are described and well documented with measurement results.**

Keywords – **EMI, noise, push-pull, ripple, spike**

I. Introduction

Switching power supplies are used to convert source voltage (battery, DC bus, mains voltage) to DC voltage used in different devices. Small size and efficiency approaching 96% made them common in every electronic device. Unfortunately, they generate unwanted noise in a form of high frequency harmonics. Therefore, measures must be taken in careful board layout, shielding, filtering and synchronization to an external clock.

II. Principle of Reducing EMI

Most of the noise generated in switching power supplies originates from power switches and diodes. Abrupt voltage and current transitions needed for high efficiency are the main causes of noise. As a result input and output voltages contain low frequency ripple from 100kHz to few MHz and high frequency content (switching spikes) with harmonics approaching 100MHz. Lowering the frequency and increasing transition times can dramatically reduce ripple and spike amplitude.

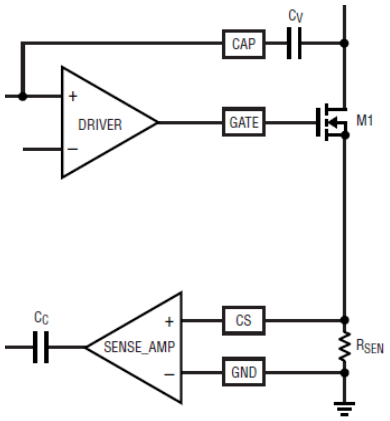

Fig.1. slew control

DC/DC controller from Linear Technology is a fixed frequency, dual output (push-pull) current mode switching regulator with unique circuitry to control the voltage and current slew rates of the external N-channel MOSFETS. The push-pull topology is desirable for low noise converters because it draws current more continuously from the input source, thus reducing the electromagnetic interference.

As seen on Fig.1 capacitor C_V provides the voltage slew rate feedback, while the current slew rate occurs by means of the sense resistor R_{SEN}. Because of the voltage slew control, MOSFET ringing is reduced and clamping circuits or snubbers are not required. The slew rates are simply adjustable through changing the values of two resistors. The trade-off between noise and converter efficiency must be made, fortunately the loss of efficiency is less than 5% in most cases.

DC/DC controller has all protection features including opposite gate lockout, soft-start, output current limit, short circuit current limit, gate drive overvoltage clamp and input undervoltage lockout.

III. Design and Analysis

The task is to design a 10W low noise push-pull converter (Fig. 2) using current mode control IC with careful choice of operating parameters and components. Achieving the lowest possible noise is the primary objective. The footprint size must be around 100x50mm.

First we choose the switching frequency to be around 75 kHz, which is a compromise between the harmonic content and size of the magnetics. Knowing that, a good choice of core for the transformer and the inductor are EFD20 and EFD15 respectively, both N87 material from TDK-EPCOS.

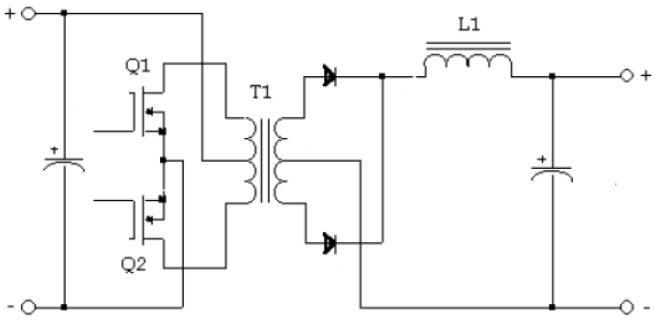

Fig.2. Push-pull converter

Design specifications are given in Table I.

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TABLE I
DESIGN SPECIFICATIONS

		Min	Typ	Max	
Input voltage	V_{IN}	18	24	36	V
Output voltage	V_O		5		V
Output current	I_O	0.2	2		A
Output current limit	I_{OCL}		2.4		A
Full load efficiency	η		75		%
Switching frequency	f_{SW}		75		kHz

Starting from design specifications we will now calculate basic parameters for the transformer and inductor (Table II).

TABLE II
BASIC PARAMETERS

		Max	Typ	Min	
Duty cycle	D	0.82	0.61	0.41	
Number of prim. turns	N_P		23		
Number of sec. turns	N_S		9		
Primary RMS current	I_{PRMS}	0.58	0.50	0.41	A
Secondary RMS current	I_{SRMS}	1.35	1.17	0.96	A
Output inductance	L		36		μH
Number of induct. turns	N		19		

Now it is time to wind the transformer and output inductor. We will use 0.35 mm enamelled copper wire for the primary and 2 parallel strands 0.4 for the secondary, in order to minimize copper losses. For the output inductor we will use 3 parallel strands of 0.4 mm enamelled copper wire.

Knowing specific core losses we can now calculate the losses in both magnetic components (Table III). Total transformer power loss at 24V input voltage is 306mW. This results in approximately 14 °C rise above ambient temperature. The temperature rise on the inductor is 7 °C. Satisfied with the results, we will keep the chosen core geometry.

TABLE III
TRANSFORMER AND INDUCTOR LOSSES

		Max	Typ	Min	
Core effect. volume	V_E		1.46		cm^3
Specific core losses	P_V		0.04		W/cm^3
Primary resistance	R_P		155		mΩ
Secondary resistance	R_S		24		mΩ
Core loss	P_{CORE}		120		mW
Primary loss	P_{PRI}	156	117	78	mW
Secondary loss	P_{SEC}	132	99	66	mW
Inductor loss	P_{IND}		160		mW

IV. REALISATION

DC/DC converter was built on four layer FR-4 substrate with 35μm copper with footprint 104x45mm. The transformer and the output inductor are wounded on through hole coil formers according to calculations. Current sense resistor is adopted for primary current sensing because of its small power dissipation (less than 40mW). Output voltage is further filtered out by the added LC filter. All electrolytic capacitors are low ESR conductive polymer aluminum electrolytic capacitors.

Using lab power supply 0-60V/3A and resistive load, we are monitoring output voltage noise and slowing down the slew rates slowly increasing the slew control resistors. As a result the noise before the LC filter is dominated by the fundamental frequency of the converter with little or no spikes at all.

Furthermore we have measured full load efficiency at various input voltages. The results are given in Table IV. The efficiency is around 75%, which is not so bad. Simultaneously with efficiency measurements we have recorded the waveforms at the point of interest.

TABLE IV
EFFICIENCY

		Min	Typ	Max	
Input voltage	V_{IN}	18	24	36	V
Input current	I_{IN}	0. 716	0.555	0.390	A
Input power	P_{IN}	12.89	13.32	14.04	W
Efficiency	η	77.60	75.00	71.20	%

The drain waveforms of primary power switch at full load and input voltages of 18, 24 and 36V are given in Figs. 3, 4 and 5 respectively. Characteristic gate voltage waveform can be seen in Fig. 6.

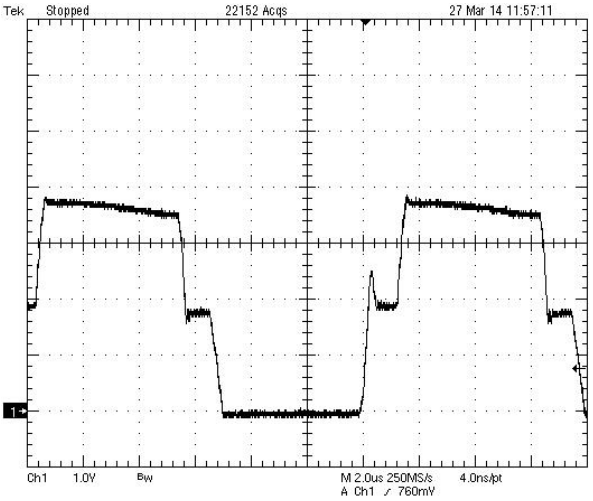

Fig..3. Drain voltage waveform at 18V

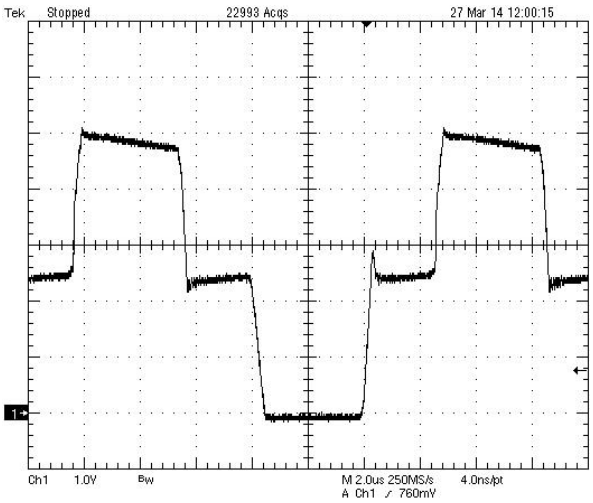

Fig.4. Drain voltage waveform at 24V

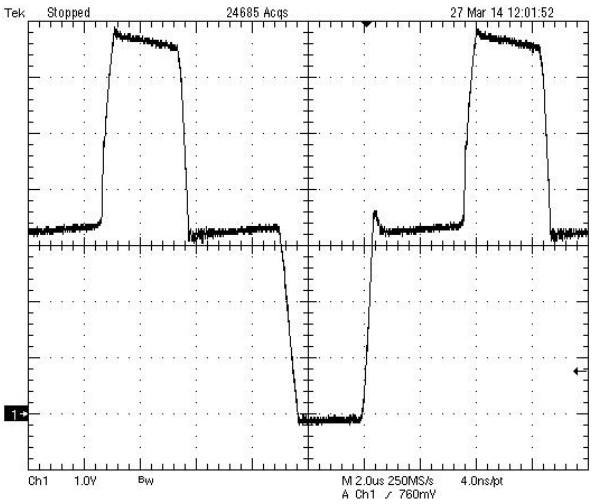

Fig.5. Drain voltage waveform at 36V

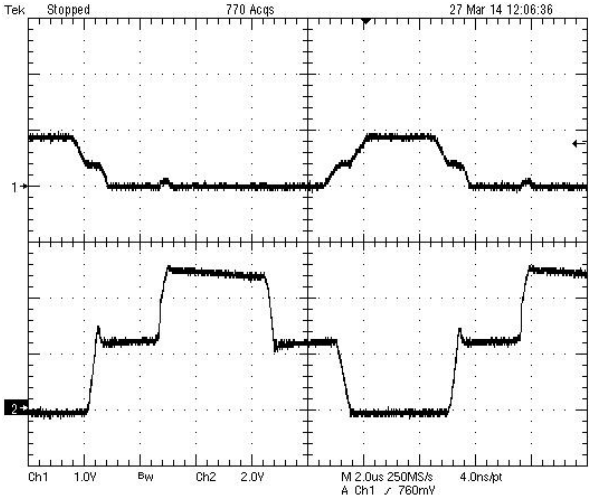

Fig.6. Drain and gate voltage waveform at 24V

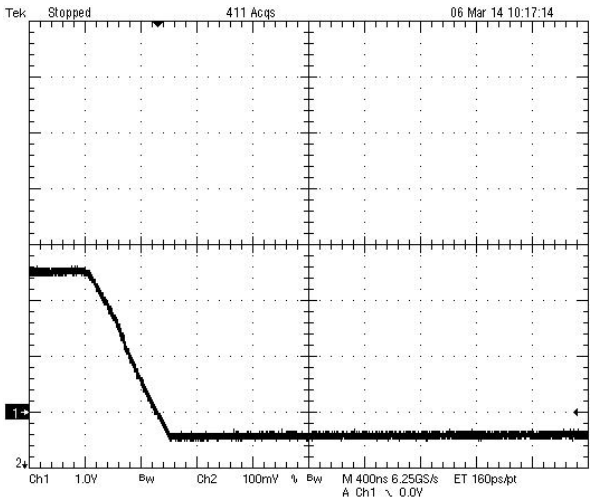

Fig.7. Drain voltage ON slew rate at 24V

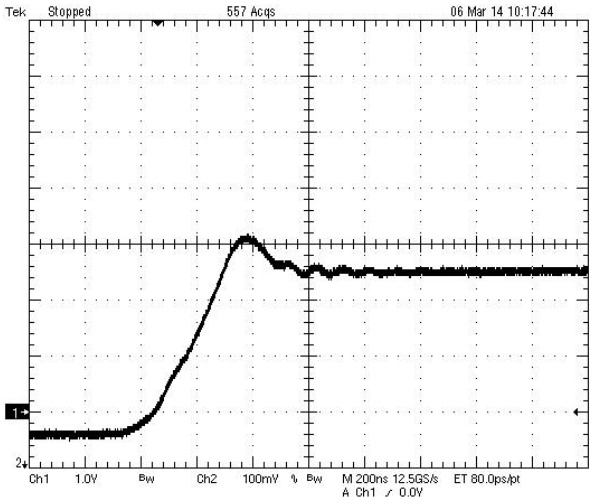

Fig.8. Drain voltage OFF slew rate at 24V

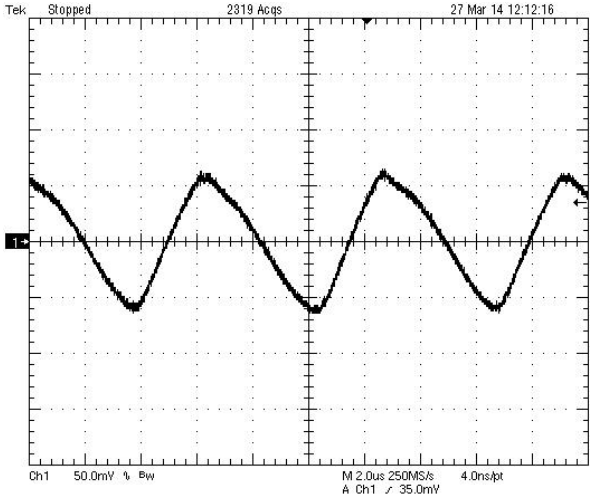

Fig.9. Input voltage ripple at full load

The edges of the square wave drain waveform are slewed to trapezoidal shape (Fig. 7 and 8). As we can see the transition times are more than 400ns (in "normal" converters usually 50 to 100ns) and the net result is low harmonic content.

The input voltage ripple is around $1V_{pp}$ (Fig.9) and contains only fundamental frequency without ugly spikes. It is a good result knowing that the input capacitor is a small 2.2µF ceramic capacitor. Small input filter can attenuate the noise to less than $5mV_{pp}$ (Fig.10).

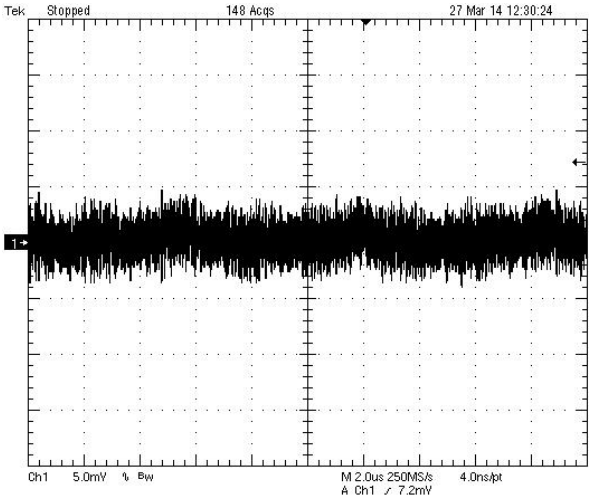

Fig.10. Input voltage ripple with small LC filter at full load

Output voltage ripple before the LC filter (Fig.11) is $5mV_{pp}$ at the fundamental frequency with $8mV_{pp}$ spikes.

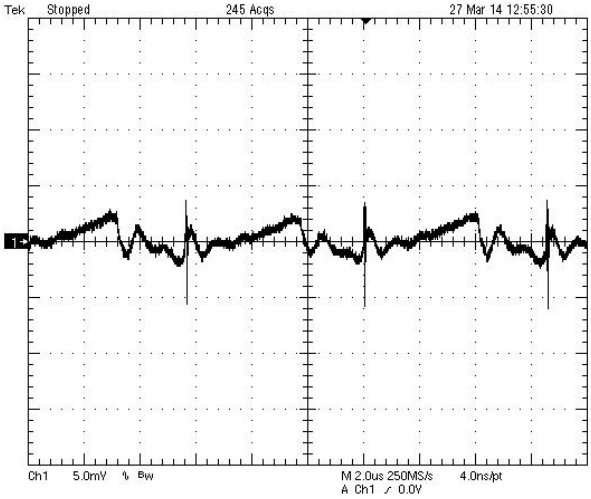

Fig.11. Output voltage ripple at full load before the LC filter

After the output LC filter the residual noise is $1mV_{pp}$ at full load and bandwidth 150 MHz (Fig.12).

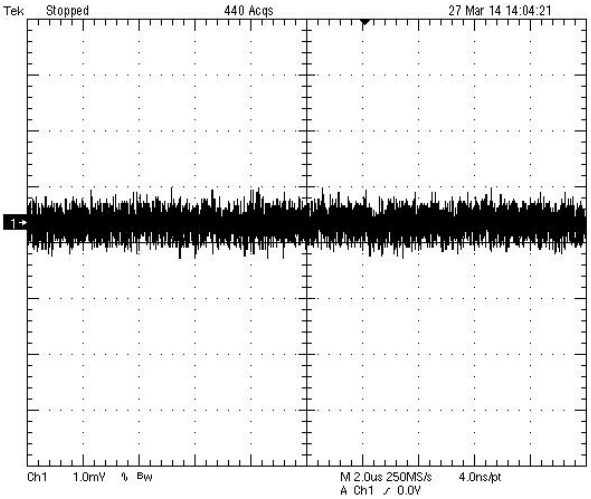

Fig.12. Output voltage ripple at full load after LC filter

The picture of converter prototype is given in Fig.13.

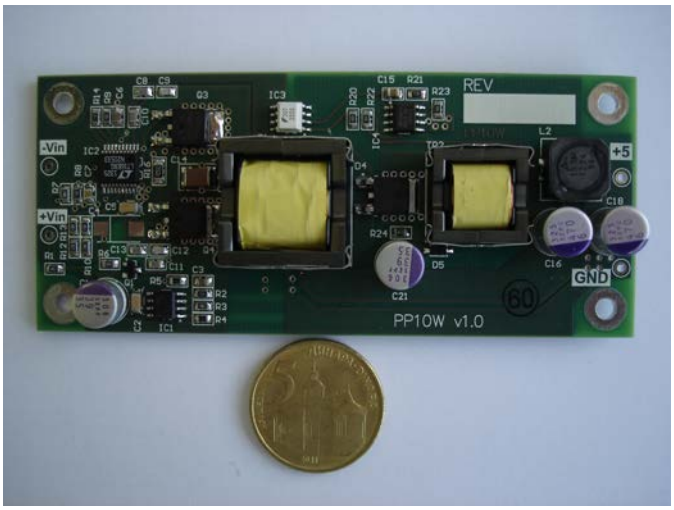

Fig.13. Converter prototype

ACKNOWLEDGEMENT

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