Verilog-A Noise Macromodel of Current Feedback Operational Amplifier with Improved Speed and Accuracy

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Abstract – **In the present paper various methods to improve the simulation speed of Verilog-A macromodels are described. For the purpose of this research, a Verilog-A macromodel of the LM6181 current feedback low noise operational amplifier is analysed and optimized. The simulation speed of the model is measured after each optimization step to assess the impact on the performance. The accuracy of the noise model is also improved by replacing the noise sources with table defined data from the datasheet.**

Keywords – **Effectiveness, Optimization, Verilog-A, Noise macromodel, Current feedback operational amplifier.**

I. Introduction

With the growth and rapid expansion of the market for electronic devices, there is a high demand to reduce the design time of new mixed mode systems and components, combining analogue and digital functions of electrical and non-electrical behavior [1]. An important part of the development process, is the verification of blocks and systems. Performing detailed and accurate tests on the entire device or large blocks from it, requires detailed models and is a time consuming process. To aid this process, optimized models may be used that require much less simulation time.

Many of the device parts have detailed *Spice* models. The digital logic is usually implemented in languages like Verilog or VHDL. Some modern simulators like *Dolphin SMASH* [2] support mixed language simulation of *Spice*, Verilog-AMS and VHDL-AMS models in the same project. The alternative is to implement the analogue and digital parts of the design in the same language. This offers a better portability, but some elements only have a *Spice* model and need to be translated to Verilog-AMS or VHDL-AMS. The rich set of functions [1], [3] in these languages eases the creation of new models at any abstraction level, from system to large and detailed models. Compared to VHDL-AMS, the Verilog-A/AMS models are faster, and easier to write and optimize. Verilog-A models are negligibly slower than their *Spice* equivalent, but the richer set of features in Verilog-A allow detailed and complex models to be optimized to achieve much better simulation times. This benefit is of a great importance for the circuit designers [4].

In the present paper a detailed Verilog-A macromodel of the LM6181 current feedback operational amplifier [5] is optimized. At each step, the speed improvement is given. The model includes noise effects. The noise accuracy is improved by using table defined noise sources from the datasheet.

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II. Improve the Effectiveness of the Model

A. Optimizing the thermal effects group

In model M_0 [5], the circuit in Fig 1a is used to model the thermal behavior, where $I_{12\text{-}14}$ are independent current sources and $R_{27\text{-}29}$ are temperature dependent resistors. The Verilog-A code in Fig 1b models I_{14}-R_{29} and uses the voltage across them as a contribution to $V(EOS)$. T_C is a function that returns the scaling factor of the resistances, depending on the difference between the device temperature and its nominal value, and the coefficients specified as parameters. The voltages in nodes $n_{55\text{-}57}$ are added to the equations of their temperature dependent signals $I(GB_1)$, $I(GB_2)$ and $V(EOS)$.

In model M_1, the circuit from Fig 1a is removed, and the equations for temperature effects, are added directly to $I(GB_1)$, $I(GB_2)$ and $V(EOS)$. Fig 1c shows the optimized Verilog-A implementation for $V(EOS)$. The old code that does not change is replaced with (**…**). The matrix order of the model is reduced by 3.

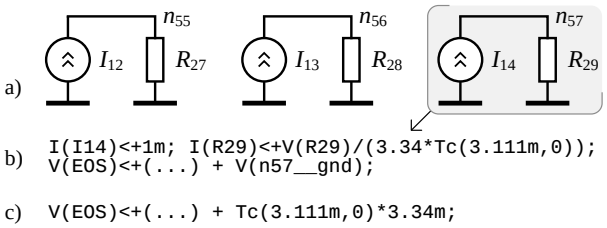

Fig. 1. Schematic (a) and Verilog-A code (b) of an auxiliary circuit for thermal effects modeling, (c) optimized code for $V(EOS)$

B. Optimization of pole stages

In model M_1, the pole stages are implemented with 5 *G*-*R*-*C* blocks, as shown in Fig 2. The voltage across R_8 drives E_H so that nodes n_{49} and n_{98} always have the same potential.

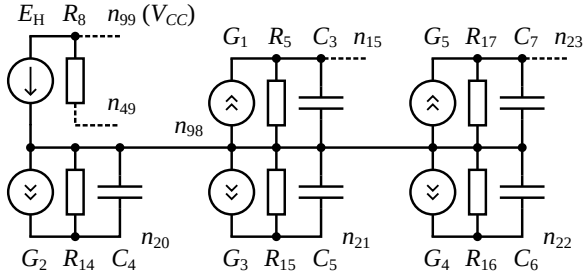

Fig. 2. Schematic implementation of the pole stages

The *R-C* groups implement pole stages; the corresponding current sources $G_{1\text{-}5}$ are controlled from the voltage across the previous. Nodes n_{20}, n_{21} and n_{22} are not connected anywhere else in the model, so only their stages can be optimized. In M_2 these stages are implemented using a Laplace function [7], reducing the matrix order by 3. Laplace is computationally expensive, and would reduce the speed of the model if used for a single stage. For many stages however, there is a benefit, because the simplified model compensates the overhead.

The source signal for the function is the voltage across G_1, the output signal drives G_5. Its gain of 1*m* is considered in the Laplace numerator. The transfer function of the three poles is:

$$A = \frac{G_2}{\frac{1}{R_{14}} + sC_4} \frac{G_3}{\frac{1}{R_{15}} + sC_5} \frac{G_4}{\frac{1}{R_{16}} + sC_6}, \quad (1)$$

where G_2, G_3 and G_4 = 1*k*; R_{14}, R_{15} and R_{16} = 1*m*Ω.

The equation can be transformed into the following form:

$$A = \frac{1}{1 + sRC_4} \frac{1}{1 + sRC_5} \frac{1}{1 + sRC_6}. \quad (2)$$

The poles of the Laplace transformation function are:

$$\frac{-1}{RC_4}, \frac{-1}{RC_5}, \text{and} \frac{-1}{RC_6}. \quad (3)$$

The following Verilog-A code implements the stages in M_2:

```
I(G5) <+ laplace_np(V(G1), '{-1m}, '{-1/(1k*692f),
          0, -1/(1k*692f), 0, -1/(1k*578.7f), 0});
```

C. Optimization of PSRR effects group

In [5], the *Power Supply Rejection Ratio* (*PSRR*) effects are modeled by the auxiliary schematic shown in Fig 3.

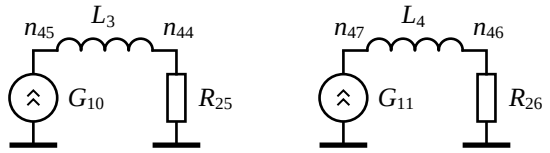

Fig. 3. Auxiliary schematic for *PSRR* effects modeling

The voltages in nodes n_{99} and n_{50} drive G_{10} and G_{11}. The voltages in nodes n_{45} and n_{47} contribute to E_{OS}.

This group may be modeled by an equation that contributes directly to E_{OS}, which reduces the matrix order of the model by 6. In model M_{3a}, it is implemented as a Laplace function, while in M_{3b}, a differential equation is used.

In M_{3a}, the *s*-domain equation has the form:

$$E_{OS} += U_{n99}(R_{25} + sL_3)G_{10} + U_{n50}(R_{26} + sL_4)G_{14}, \quad (4)$$

where: U_{n99} and U_{n50} are the potentials in nodes n_{99} and n_{50}. A Laplace function with numerator: {*R*, *L*} and denominator: {1} is used. The following Verilog-A code is used by M_{3a}:

```
V(EOS) <+ ...
+laplace_nd(V(n99__gnd),'{10,26.53u},  '{1})*141.3u
+laplace_nd(V(n50__gnd),'{10,2.27364u},'{1})*141.3u;
```

In *time*-domain, the following equation is used for M_{3b}:

$$E_{OS} += \left[\frac{dU_{n99}}{dt}L_3 + U_{n99}R_{25}\right]G_{10} + \left[\frac{dU_{n50}}{dt}L_4 + U_{n50}R_{26}\right]G_{14}. \quad (5)$$

The following Verilog-A implementation is used in M_{3b}:

```
V(EOS) <+ ...
+(ddt(V(n99__gnd))*26.53u  +V(n99__gnd)*10
+ ddt(V(n50__gnd))*2.27364u+V(n50__gnd)*10)*141.3u;
```

D. Merging of elements connected in parallel

Parallel branches defined with their *Y*-matrices can be described as a current contribution of all currents through the original branches. The matrix order remains the same, but the Verilog-A equations are reduced and the simulation speed is slightly increased. The list of branches that are optimized is shown in Table 1. The following Verilog-A code shows the changes to merge branches G_{I1} and F_{I1} from M_3 to F_{I1} in M_4:

```
M3: I(GI1) <+ 243.75u + V(in)*2.708u;
    I(FI1) <+ I(va3)*100;
M4: I(FI1) <+ 243.75u + V(F6)*2.708u + I(va3)*100;
```

TABLE I
LIST OF MERGED BRANCHES

Branches from M_3	Combined branch in M_4
in, I_2, F_6	F_6
G_{I1}, F_{I1}	F_{I1}
G_{I2}, F_{I2}	F_{I2}
G_{R6}, G_{B1}	G_{B1}

Branches from M_3	Combined branch in M_4
C_{IN1}, F_{N1}	F_{N1}
C_{IN2}, F_{N2}	F_{N2}
G_1, R_5, C_3	G_1
G_5, R_{17}, C_7	G_5

E. Merging of V-R and V-V elements connected in series

Voltage sources connected in series can be replaced by a voltage contribution equal to the sum of the original voltages. The *V-R* elements connected in series are changed to an equivalent *I-R* branch [7]. The list of branches that are optimized is shown in Table 2. The matrix order of the model is reduced by 6. The following Verilog-A code shows the changes required to merge V_1-R_{E1} to I_{RE1}:

```
M4: V(V1)   <+ 0.3;    I(RE1) <+ V(RE1)/130;
M5: I(IRE1) <+ (V(IRE1) - 0.3)/130;
```

TABLE II
LIST OF MERGED BRANCHES

Elements from M_4	Combined branch in M_5
V_1, R_{E1}	I_{RE1}
V_2, R_{E2}	I_{RE2}

Elements from M_4	Combined branch in M_5
E_1, V_{A8}, R_{35}	I_{R35}

F. Improved implementation of group D_8, F_5, D_7, V_{A7}

In [5], the voltage source V_{A7} is only used to obtain the current through D_7, which is output and drives F_6, Fig 5.

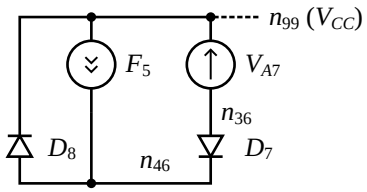

Fig. 5. Group D_8, F_5, D_7 and V_{A7}

The current through E_1 is input and drives F_5. Depending on its direction, this current flows through one of the diodes D_7 or D_8. As a result, when the current from n_{40} to n_{99} is positive, it is fed directly to the output F_6, otherwise the output current is zero. The group from Fig 5 is equivalent to the following Verilog-A implementation, which reduces the matrix order of the model by 5:

```
I(F6) <+ max(I(IR35),0) + 4.47m;
```

G. Merging of elements D_5, V_5, D_6 and V_6

In [5], diodes D_5 and D_6 are using a simplified model that can be described by the following equation:

$$I_D = I_S \exp\left(\frac{V_D}{V_T N}\right), \quad (6)$$

where I_D is diode current, I_S is saturation current, V_D is diode voltage, V_T is thermal voltage and N is emission coefficient.

Voltage sources V_5 and V_6 apply an offset to V_D. The currents of the two diodes have opposite directions and are subtracted from each other.

The complete equation that describes them is:

$$I_{DZ5} = I_{SX}\left[\exp\left(\frac{V_{DZ5} - V_{Z5}}{V_T N}\right) - \exp\left(\frac{-V_{DZ5} - V_{Z5}}{V_T N}\right)\right], \quad (7)$$

where I_{DZ5} is the combined current, V_{DZ5} is the voltage between nodes n_{40} and n_{23}, $I_{SX} = 1fA$, and $V_{Z5} = 5.3V$.

The optimized Verilog-A code reduces the matrix order of the model by 4 and has the following form:

```
I(DZ5) <+ Isx*(limexp(( V(DZ5) - Vz5)/(N*$vt))
             - limexp((-V(DZ5) - Vz5)/(N*$vt)));
```

H. Diodes with voltage source connected in series

In [5], the built-in diode model is used which is slightly faster than its equivalent Verilog-A implementation, but when combined with a voltage source in series, the built-in model is slower than a *V-D* couple modeled by a single equation. The list of elements that may be optimized is shown in Table 3.

TABLE III
LIST OF MERGED BRANCHES

Elements from M_7	Combined branch in M_8
V_{A3}, D_{S1}	D_{S1}
V_1, D_1	D_{Z1}
V_2, D_2	D_{Z2}

Elements from M_7	Combined branch in M_8
V_{A4}, D_{S2}	D_{S2}
V_3, D_3	D_{Z3}
V_4, D_4	D_{Z4}

Voltage sources $V_{1\text{-}4}$ apply an offset to V_D, while V_{A3} and V_{A4} are used to obtain the currents through the diodes. Note that V_1 and V_2 may be merged either to R_{E1} and R_{E2} as in M_5 or to D_1 and D_2 as described here, the simulation speed is the same. The following optimized Verilog-A code models D_{Z1}:

```
I(DZ1) <+ Isx*(limexp((V(DZ1)-0.3)/(N*$vt)) - 1.0);
```

I. Diode equations with improved efficiency

If the device temperature is constant during a transient simulation, the following expression is also constant:

$$NVt\_ = \frac{1}{V_T N}. \quad (8)$$

It may be used to speed-up the computation of the diode equations. In Verilog-A, a parameter *NVt_* is defined and used in the diode equations as shown in the following sample:

```
parameter real NVt_ = 1/(N*$vt);
I(DZ4) <+ Isx*(limexp((V(DZ4)+2.0)*NVt_) - 1.0);
```

III. ACCURACY OF THE NOISE MODEL

When modeling the noise behavior of a low-noise opamp, the output noise is referred to the inputs of the device [5], and the rest of the model is described as a noiseless block.

In [6] the referred noise sources generate white and flicker noise to approximate the noise characteristic of the device. Some elements are modeled as noisy and may affect the noise behavior of the model. In this step, they are replaced with noiseless equations to avoid this problem, while the noise sources are defined using tables obtained from the datasheet.

IV. EFFECTIVENESS ASSESSMENT

To assess the effectiveness of the optimized models, *AC*, *noise* and *transient* simulations have been performed on a circuit consisting of seven non-inverting amplifiers, in the environment of Dolphin SMASH [2]. The simulation times have been measured at each step. The following simulation settings are used: AC interval [1*Hz*-1*GHz*], 10*k points/decade*, and Print interval for noise contribution table: every 5^{th} point. For *transient*: Run to time 25*ns*, Print step 1*ns*, min time step 1*fs*, max time step 1*ns*, Integration method *TRAP*.

The simulation times are measured by an automation script and a custom plugin that runs in the simulator and uses API (*Application Programming Interface*) to hook simulation start and end events. The *RDTSC* processor instruction is used to

perform time measurements with a very-high precision. In the simulator exclusive mode is enabled. Real-time priority is used for the task, and the affinity is locked to a single CPU core of Intel i7 930. Hyper-threading, power saving and speed reduction features are disabled, and all simulations are run from a RAM disk to produce accurate time measurements. This resulted in a maximum deviation time less than 0.1% from the mean value. To further enhance the precision, 16 simulations are run in each case and the 8 times resulting in the lowest deviation are averaged to calculate the mean time.

The speed improvement at each optimization step for *AC*, *noise* and *transient* analyses is shown in Table 4, where $\Delta\varepsilon$ is the order reduction of the model matrix, and all values are in percent relative to the previous step.

TABLE IV
SPEED IMPROVEMENT AT EACH OPTIMIZATION STEP

Step	Δε	AC	Noise	Transient
1	3	101	101	104
2	3	110	105	101
3_a	6	103	101	96
3_b	6	114	104	102
4	0	104	103	103
5	6	105	102	107
6	5	113	109	520
7	4	120	116	109
8	8	113	132	112
9	0	101	102	101
Total	35	214	195	760

Optimizations steps 1, 3_b and 4-9 simplify the model by merging elements or equations together. As a result the simulation speed is increased for all analysis types.

Optimization steps 2 and 3_a replace element groups with equivalent Laplace transformations and simplify the model, but Laplace is heavy computationally this also introduces a negative impact on the performance. For *AC* and *noise* analyses, this effect is smaller than the performance improvement from removing multiple elements and nodes and as a result the overall simulation speed is increased. For *transient* analysis however, the negative impact is much higher and in M_{3a} it cannot be compensated, so the simulation speed is reduced. In M_2 the performance penalty for transient simulations is compensated, but the speed gain is negligible.

Step 3 has two variants: in M_{3a} the *transient* speed is reduced. Variant M_{3b} is faster for all simulation types.

With the original model [6], convergence problems were encountered for D_7 and D_8, during transitions of their currents around 0. This causes time-step reduction and has a major impact on the effectiveness of the model. Step 6 resolves this issue and improves the stability of the model. The affected block is replaced with a more simple and reliable equivalent implementation.

Optimization step 10 improves the accuracy of the noise model, by replacing the original interpolated noise behavior with table defined values from the datasheet. The noise model was verified and matches the datasheet characteristics.

V. CONCLUSION

A Verilog-A macromodel of the LM6181 current feedback low noise operational amplifier is analysed and optimized. The optimized model is 214% faster for *AC*, 195% faster for *noise*, and up to 760% faster for *transient* simulations, compared to the model from [5]. The large improvement for transient simulations comes from the removal of a block that caused instability and time-step reduction in the original model. The simulation speed of the model is measured after each step of optimization, in order to assess its impact on the performance. The model accuracy is not affected.

The optimization steps affect: thermal effects group, pole stages, *PSRR* effects group, merging of parallel elements, merging of serial elements, removal of voltage sources by transforming serial *V-R* groups to parallel *I-R* and moving the voltage source from *V-D* groups connected in series to the diode equation as an offset voltage.

Although replacing large blocks with a Laplace function improves the speed of the model, for smaller blocks the negative impact from Laplace computation on the speed, particularly in the *time*-domain, may be higher than the speed improvement from the reduced number of elements and equations and should be avoided.

Due to the restricted set of features in the *Spice* language, many models use inefficient solutions to perform simple tasks. These blocks may be entirely rewritten and optimized using the advanced features of Verilog-A, to improve the simulation speed and stability without sacrificing any accuracy.

The noise accuracy of the model is enhanced by replacing the noise sources with table defined data from the datasheet. The noise model was verified and matches the datasheet data.

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