Based on CPLD Programmable Counter for Experimental Digital Electrical Energy Meter Part 2

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Abstract – **A creating of digital electrical energy meter conduces to its correctly measurement and to a price fixing of each electronic setup. Each measuring device effectiveness increases considerably with a introducing in them of modern programmable setup. The article presents a module depicting a electrical energy measurement information received by developed digital three-phase electrical energy meter The block diagram of the device, the principle circuit diagram display and programmable logic have been presented. The schematic diagram of the counter programmed into the programmable block has been presented. The timing diagrams describing the operation of the device have been presented. The described module has real application in different digital electricity meters. The counter allows flexibility in the programming of reading programme.**

Keywords – **Programmable logic device, CPLD, FPGA, Digital measuring device.**

I. INTRODUCTION

A modern measuring device improvement increases an accuracy, reliability decreases operator participation and measuring and indication time leads to automatic adjustment, self test, lower production and market prices. This all is possible with a modern programmable integrated circuit introduction based on CPLD and FPGA structures. Almost each up-to-day electronic device has reprogrammable module permitting not only flexible fulfilling of a measuring algorithm but also and a possibility to renovate managing software with an aim to get bigger efficiency and functioning. Reprogrammable logical set or more accurate programmable logical matrixes are more applied in an industry, motor-car and medical electronics, telecommunications, instrumentation etc. Their application in devices for consumption and generation measurement for instant of water, electrical energy increases a device reliability and a measured parameters keeping for a longer time [1-6].

An experimental development of electronic counter for three-phase electrical energy meter is described in the article. It is realized on the base of produced by Xilinx® integrated device CPLD and rules six digit seven segments LCD.

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II. PRESENTATION

The created programmable counter block schematic diagram is shown in Fig. 1.

Its main component is a programmable unit PLU. It is built by a produced by Xilinx programmable logical device CPLD of the family XC9572. The logical device program is ushered by an external personal computer by means of IEEE1149.1 interface, known as JTAG. The described further software arranges input-output pins in such manner so and the information about enumerated units have to come energy measuring device in a strictly determined by a clock generator (G) time. In the same time the information about enumerated pulses is depicted in six digit seven segments LCD ruled by six CMOS decoders (D1-D6). The signals from EM get across input buffer in order to protect the matrix inputs. The measured information is preserved by means of transmission through communication port (CP) to an additional memory.

The unit for information displaying DU is another big module. It is consist of six decoders D1-D6 and six digit LCD. The circuit power supply is by a unit PU giving electrical voltages for separate blocks – logical matrix, decoders and pulse generator (U_{DD} = 5V) and negative voltage (U_{EE} = -5V) applied to a decoder for display control.

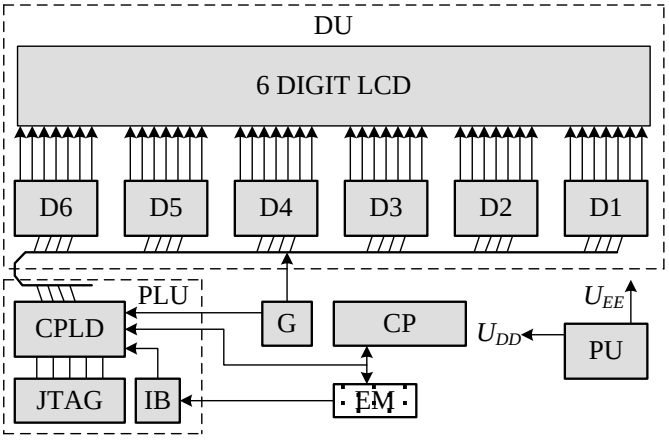

Fig. 1. Functional block diagram of programmable counter

A display module schematic circuit diagram is depicted in Fig. 2.

It is realized on base of six CMOS decoders (IC4 ÷ IC9) of the type CD4055. They control six digit seven segments LCD indicator. To each of decoders a negative U_{EE} = -5V voltage to pin 7 is applied and alternating with 200Hz frequency signal to pin 6 for correct display control. All unused pins are switched to ground. It is not depicted in Fig. 2.

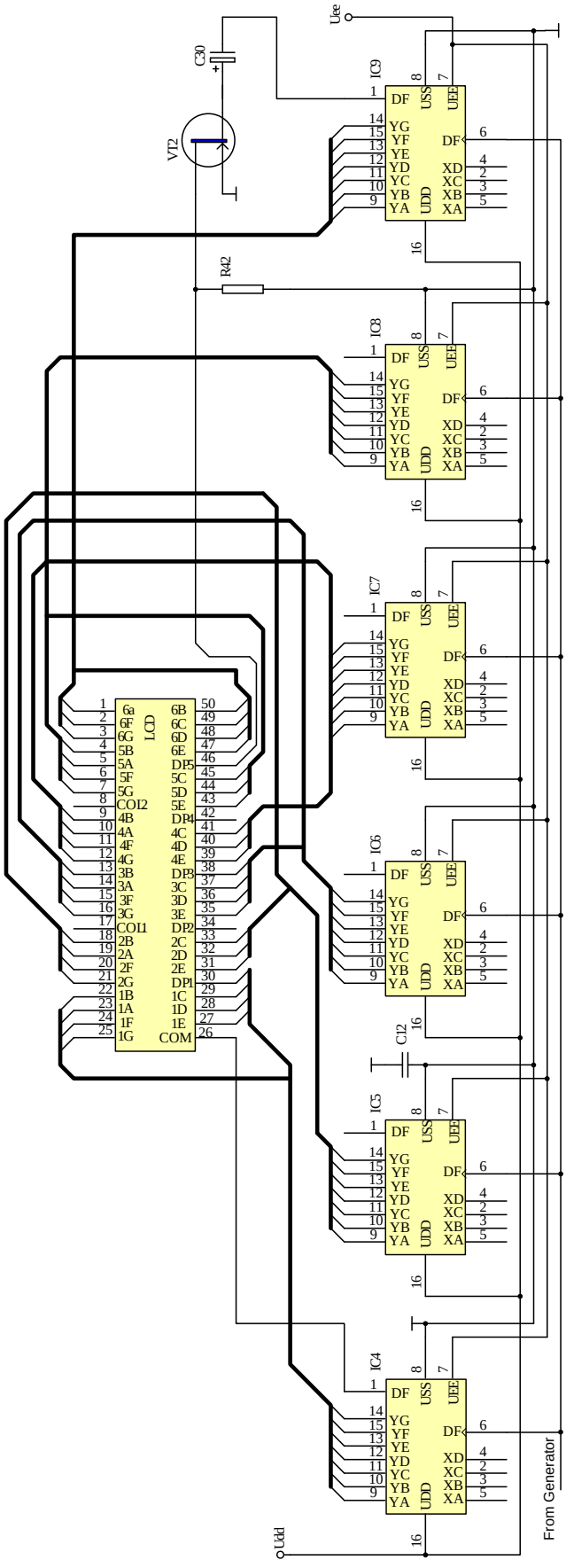

Fig. 2. Display module schematic circuit diagram

A schematic circuit diagram of programmable logical unit PL is shown in Fig. 4. It is created on the base of a produced by Xilinx programmable logical matrix. The matrix IC3 is produced in case PQFP-84 and is of the type XC9572 and enables programming according to conventional IEEE1149.1 interface. The circuit IC3 more leads are taken out to connectors.

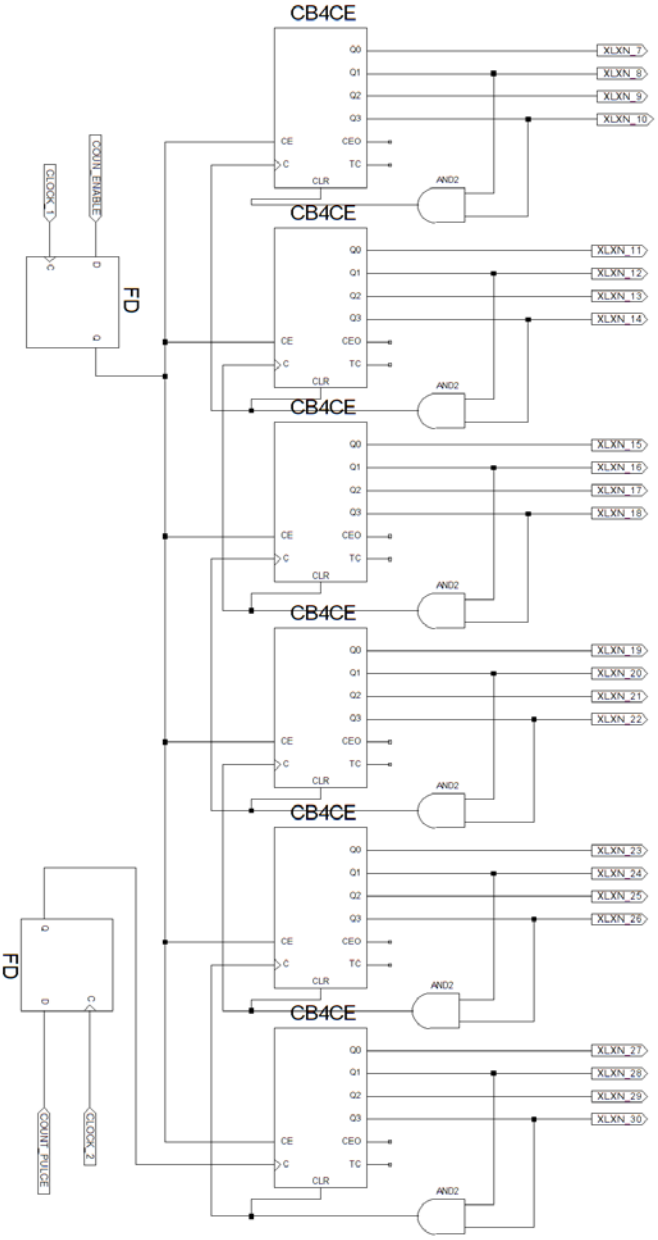

Fig. 3. Schematic circuit diagram of counter

It enables additional modules switching and device functional possibility extension. Another leads receive signal extra amortized by a logical element NAND with ordinary input (IC2 – CD4011 from port CON B) and with Schmitt trigger on an input (IC11 – CD4093 from CON 4). By means of connector CON 1 a personal computer makes a device program. A schematic circuit diagram of a unit G is realized on the base of integrated generator of the type LM555

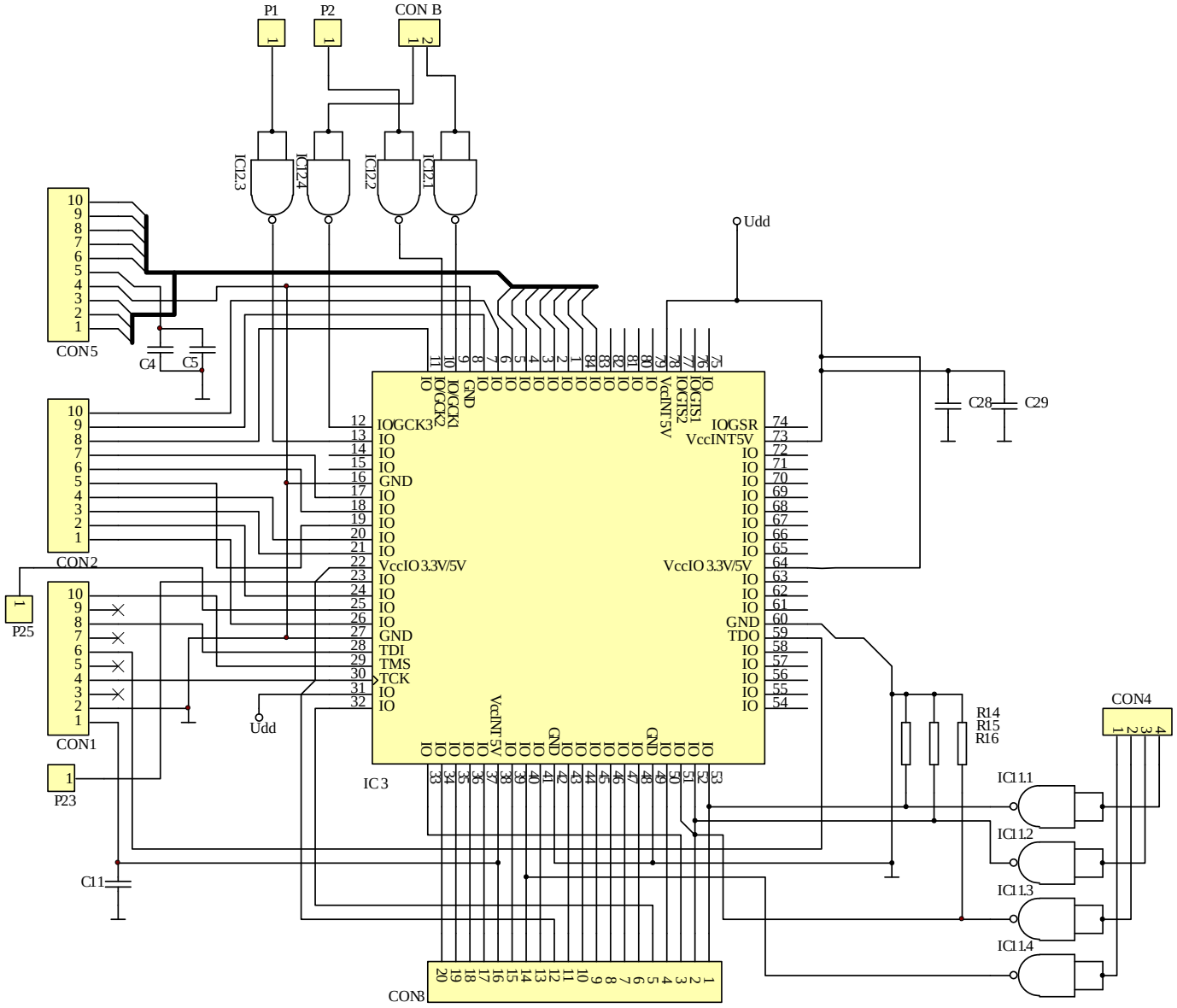

Fig. 4. Schematic circuit diagram of programmable logical unit

switched as a mono-stable multivibrator. The generated by this circuit pulses are used only for LCD control and are fed to pins 6 of the decoders (IC4÷IC9). This signal is too used by unit PLU for a noise stability increase of a circuit work. These circuit elements are so selected and output frequency is 200Hz. In Fig. 5 is shown a schematic diagram of generation circuit, realized by integrated generator of the type LM555.

The soft ware is realized by program product Xilinx ISE10.1. The used in the device program schematic circuit diagram is as for an ordinary counter but it is possible to create more complex one with more functions. The complete circuit diagram consisted of 6 switched in series binary-decimal counters is depicted in Fig. 3.

By means of a logical element AND they are connected. So they receive a high level (logical “1”) at a passage from 9 to 10 and a lower digit gets to zero, The generated by integrated circuit EM pulses with alternating duration are fed to D–trigger through a terminal COUNT PULSE configured to pin 9 of EM. A high frequency signal from a configured as an input pin 10 of circuit IC3 is fed to a clock input C of a D-trigger of EM through a terminal CLOCK2. This signal is received from a generator unit. After this manner a noise perception is avoided and it can not be counted as useful signal.

A permissive circuit configuration created by another D-trigger is the same.

The measuring electrical energy unit has time at a working setting up by a first switching or by a power supply temporarily interruption indicated by the light of LED RP. The programmed in a matrix IC3 counter starts to count upon the permuting signal receipt (logical “1”) from integrated circuit IC2 (electrical energy meter) lead REVP. This signal is applied to terminal COUNT ENABLE through integrated

circuit IC3 pin 13. A high frequency signal from a pulse generator is applied to terminal CLOCK 1.

Timing diagrams describing the operation of the module are shown in Fig. 6. They indicate the status of the output ports of the programmable matrix at the time of the input signal. Fig. 7 shows a waveforms of display depolarizing signal and the main generator signal.

When the device is switched off or the power supply is interrupted the accumulated up to this time values do not keep. If the power supply is restored the counter will begin to count from zero. It can be avoid by means of an additional in program diagram block which sends data to a externally memory. The connectors CON 2, CON 3 and CON 5 of the printed circuit board are provided for an external switching of EEPROM or other device for control and data acquisition. The last is not described in this paper.

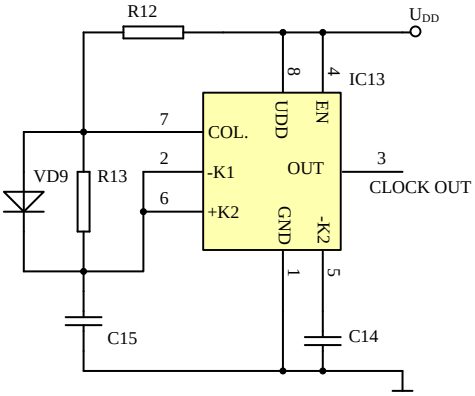

Fig. 5. Schematic circuit diagram of pulse generator

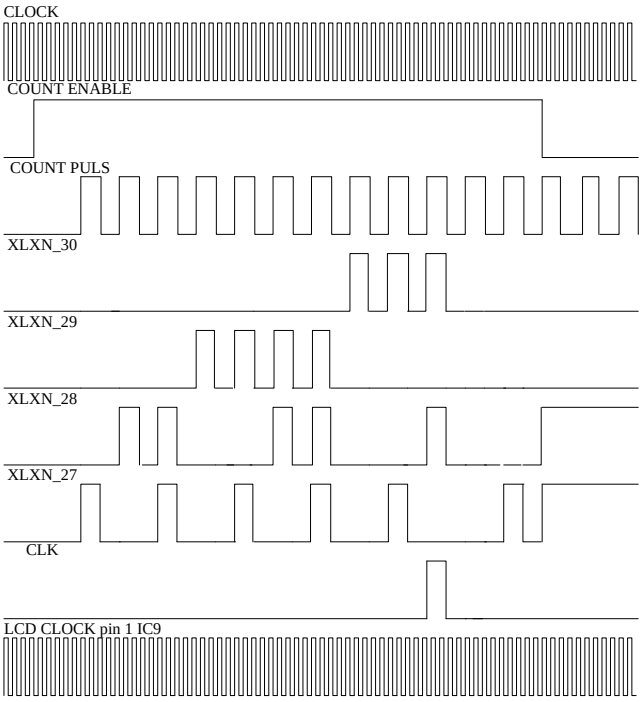

Fig. 6. Timing diagrams describing the operation of the module

III. CONCLUSION

A functional block schematic diagram and a schematic circuit diagram of a programmable counter on the base of a programmable logical matrix XC9572 is synthesized.

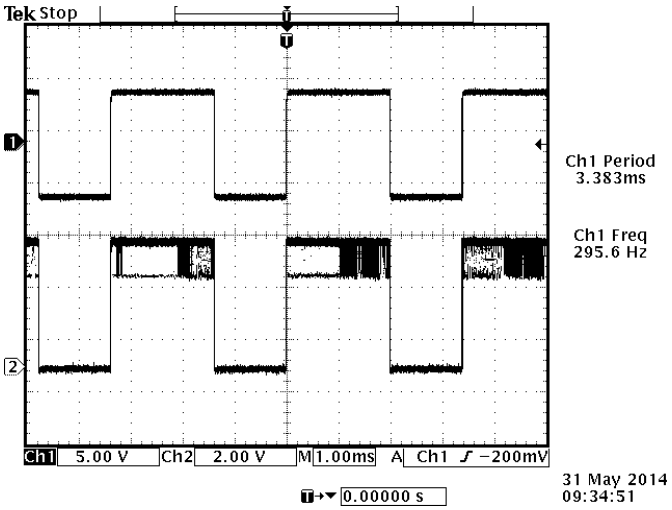

Fig. 7. Waveforms of depolarizing LCD signal versus clock signal

The described module is expected to be further developed with the addition of memory and design of different tariffs for reading.

The realized elaboration application is to count pulses generated by a three-phase electrical energy meter but it can be use in another similar cases.

The developed module for counting pulses from a digital electricity meter offers flexibility in designing. Using the capabilities of the produced by company Xilinx programme environment ISE10 the programme has can be made by program language C or by schematic editor. This enables designers with a bad programming experience, but knowing better circuitry to cope with such task.

The realized circuit decision priority is accessible and cheap elements embedding which do not require an electrical energy big consumption and special software knowledge.

REFERENCES

[1] T. Angelova, “Experimental Device for Automation Reeding of Galvanomagnetic Elements Transduser Characteristics”, Journal of the Technical University of Gabrovo, Vol. 44, 2014.

[2] N. Draganov, “Based of AMR Sensor Device for Contact less Measuring of AC Current”, Journal of the Technical University of Ruse, Vol. 52, series 3.1, Ruse, 2012, pp. 66-70.

[3] N. Draganov, “Contactless protection of induction motor”, Scientific Works Volume LX, Food Science, Engineering and Technologies – 2013, 18-19 October 2013, Plovdiv.

[4] Analog Device, Application notes and part information, www.analog.com, Jan. 2014.

[5] N. Draganov, “Integrated Evolution Sistem for Programmable Sensors Signals Conditioner of ZMDI Company”, Journal of the Technical University of Gabrovo, Vol. 44, 2012, pp. 42-47.

[6] Xilinx, Application notes and part information, www.xilinx.com, Jan. 2014.