# Three-Phase Soft-Switched Quasi Resonant DC Link Inverter for Induction Motor Drive Application

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Abstract – A zero-voltage transition soft-switching inverter for an induction motor drive is developed. The proposed softswitching inverter is formed from the traditional pulse-width modulated (PWM) inverter by simply augmenting with auxiliary resonant circuits, and the soft switching is achieved through applying PWM switching control signals with suitable delays for the switches. The designed soft-switching inverter is used for powering an induction motor drive to test its effectiveness. The proposed drive system is modelled and its performance is simulated in PSpice. The simulation results show that a smaller switching loss and higher conversion efficiency are obtained by the proposed soft-switching inverter.

*Keywords* – Induction motor drive, Soft-switching inverter, Zero-voltage transition.

### I. INTRODUCTION

Inverters have many applications in power electronic devices. The performance of a pulse-width modulated inverter-fed system can be much improved by increasing the switching frequency. In hard switching inverters, a higher switching frequency leads to increased switching losses which consequently increases the size of the snubber circuits [1, 2]. This will suffer by giving large switching stresses of the power devices. In addition, electromagnetic interference increases and efficiency decreases. To overcome these problems, the application of soft switching techniques is essential [1-5].

The resonant DC-link inverter is the most commonly used one for induction motor drives, owing to its simplicity, but it possesses the disadvantage of having a high resonant link voltage, which is equal to or greater than twice the supply voltage [1].

Quasi-resonant (QR) inverters offer several advantages compared with resonant DC-link inverters with regard to resonant link design and control, device rating requirements and use of pulse width modulation (PWM) [6]. The QR inverter schemes generate zero-voltage instants in the DC link at controllable instants that can be synchronised with any PWM transition command, thus ensuring a zero-voltage switching condition of inverter devices. As a result, these inverters can be operated at high switching frequencies with high efficiency [6].

The passively clamped QR inverter is reported in [7]. This

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<sup>2</sup>Nikolai Komitov is with the Department of Electrical Engineering, University of Food Technologies - Plovdiv, 26, Maritza Blvd., 4002 Plovdiv, Bulgaria, e-mail: nikkomitov@abv.bg topology satisfying most of the essential requirements, such as low clamp factor, simple resonance control, guaranteed zerolink voltage condition, PWM capability, use of only one auxiliary switch and recycling of resonant energy. The only drawback of this scheme was the high reverse voltage requirement of the clamp diode. This problem can be solved by use of a separate, low-voltage DC source [5, 6]. Another possible solution could be to use a simple R-C parallel circuit to maintain low voltage [6].

One of the main QR inverter research goals is to achieve soft switching conditions with a minimum number of auxiliary circuit elements [2]. Reducing the number of auxiliary switches simplifies the control circuit and decreases the inverter cost.

The object of this work is to develop and simulated in PSpice a tree-phase induction motor drive fed by a PWM voltage source soft-switching inverter. It is necessary to investigate a performance of proposed drive system for the dynamic and steady-state modes.

## II. SIMULATION MODEL

The circuit diagram of the QR inverter is illustrated in Fig. 1. This topology is similar to the classic converter, plus an auxiliary circuit consists of switch  $S_a$ , antiparallel diode  $D_a$  and the coupled inductors  $L_{r1}$  and  $L_{r2}$ . The dc-link switch is  $S_L$  and the dc-link resonant capacitor is  $C_r$ .



Fig. 1. QR DC-link inverter

The circuit operates by setting up a resonating dc link that periodically returns the dc bus voltage to zero. During the interval that the diodes in antiparallel with the main inverter devices are conducting, all inverter devices may be turned off, if desired, with minimal turn-off losses. At the same time, all incoming devices may be turned on with zero turn-on losses.

Six operating intervals can be identified. Before the first operating interval, it is assumed that  $S_L$  is on and  $S_a$  is off. This regime corresponds to the pseudo steady state conditions with link voltage equal to  $U_s$ . The output current  $I_o$  flows through  $S_L$ 



Fig. 2. Resonant link waveforms

Whenever a change in the state of the inverter main switches is desired,  $S_a$  is turned on  $(t_1)$ . Due to existence of  $L_{r1}$ , the turn on of  $S_a$  is under zero-current switching condition and  $i_{sa}$  increases linearly  $(t_1 \div t_2)$  until it reaches  $I_{min}$  which is defined as the minimum required current of  $L_{r1}$  that guarantees the charging of  $C_r$  in interval  $(t_4 \div t_5)$ . The design procedure of  $I_{min}$  is illustrated in [2].

When  $i_{sa}$  reaches  $I_{min}$ , switch  $S_L$  must be turned off  $(t_2)$ .  $S_L$  is turned off under zero-current switching condition due to the existence of  $C_r$ . In this interval, a resonance starts between  $C_r$  and  $L_{r1}$  which decreases the dc-link voltage  $(t_2 \div t_3)$ .

When  $u_{cr}$  reaches zero the diode  $D_a$  turns on  $(t_3)$ . Thus, a fraction of the flux linkage of  $L_{r1}$ , moves to  $L_{r2}$ . In order to operate at zero-voltage switching condition, the state of the inverter switches must be changed in this interval  $(t_3 \div t_4)$ . After the inverter switches change state, switch  $S_a$  then turned off in a zero-voltage switching manner  $(t_4)$ . Thus,  $i_{da}$  current increases and begins to charge  $C_r$   $(t_4 \div t_5)$ .

When  $C_r$  reaches  $U_s$ , antiparallel diode of the switch  $S_L$  turns on under zero-voltage switching condition (t<sub>5</sub>). Thus, switch  $S_L$  can be turned on under zero-voltage-zero-current switching condition.  $i_{da}$  current decreases to  $I_o$ . When the antiparallel diode of the switch  $S_L$  current reaches zero and turns off under zero-voltage-zero-current switching condition, the  $S_L$  current begins to increase until it reaches  $I_o$  and  $i_{da}$  current reaches zero (t<sub>6</sub>).

After this interval, the link returns to the pseudo steady state and the cycle repeats for the next switching command.



Fig. 3. Control circuit diagram for soft-switched PWM modulation

#### **III. RECEIVED RESULTS**

Simulation is done on a three phase induction motor fed by a PWM inverter developed in PSpice. The basic circuit of the proposed scheme consists of a three phase induction motor type AO-90S-4 having ratings as 1,1kW, 380V, 50 Hz which is connected to drive the constant nominal load. The PSpice model of three phase induction motor inverter drive has been developed in [7]. The technical data of the electric motor are given in Appendix.

The design of the proposed inverter involves the selection of parameters  $C_r$ ,  $L_{r1}$ ,  $L_{r2}$  to satisfy the desired link waveform specifications such as du/dt, di/dt and peak currents [6]. The design expressions are derived from the differential equations of each mode of the resonant cycle [1-7]. A set of parameters has been chosen as  $L_{r1}=10\mu$ H,  $L_{r2}=10\mu$ H,  $C_r=10n$ F. The magnetic coupling between  $L_{r1}$  and  $L_{r2}$  is designed as 0.9.

A three-phase sine-triangle PWM command generator was implemented to control the six inverter switches. The frequency of the carrier wave is maintained at 2 kHz.

Inverter control is implemented based on the link operation requirements, whenever a switching signal is generate, the auxiliary circuit must first be turned on to initiate a resonant transient. The inverter switches, when the link voltage reaches zero. A block diagram for a control scheme is shown in fig. 3. The edge detector locates the desired state change before the switching command is passed to the inverter switches. The detected edges are used as an input of a RS-flip flop to turn on of the auxiliary circuit. The auxiliary switch turns off, when the state of the inverter switches was changed. When  $i_{sa}$  reaches  $I_{min}$ , the pulse is used as an input of a RS-flip flop to turn of  $C_r$  reaches  $U_s$ .

Fig. 4 shows the link voltage  $u_{DC}$ , inverter line-line voltage and phase current. It is seen that there is some distortion in the motor current. The reason for the distortion has to be attributed to the minimum link pulse requirement in the resonant inverter.



Fig. 4. Dependences  $u_{DC}$ ,  $u_{AB}$ ,  $i_A = f(t)$ 

From the basic waveforms shown, it is seen that some limitations still exist. The control circuit must drive the auxiliary switch and the dc-link switch at the proper time. It can be observed from Fig. 2, that the state of the inverter switches can be changed 1µs after turning  $S_L$  off. When the control circuit decides to change the state of inverter switches, this action should be performed with a delay 0.6µs in order to have enough time to reduce the dc-link voltage to zero. Thus, switch  $S_a$  is turned on first and  $i_{sa}$  current increases until it reaches  $I_{min}$ . This current must be large enough ( $I_{min}$ =26.8A) to guarantee charging  $C_r$ . A larger  $I_{min}$  causes greater current stresses on  $S_L$  and  $S_a$  [2].

The fall time for the link voltage is about 990ns. The zero link voltage condition maintained for about  $1.3\mu s$ . The rise time for the link voltage is more than  $1.7\mu s$ .



Fig. 5. Dependences  $u_{CE1}$ ,  $i_{C1}$ ,  $p_{S1} = f(t)$  with "soft switching" control scheme



Fig. 6. Dependences u<sub>CE1</sub>, i<sub>C1</sub>, p<sub>S1</sub> =f(t) without "soft switching" control scheme

Management of inverter drives attached proposed control algorithm for "soft switching" voltage of the keys. Fig. 5 shows the shapes of the current, voltage and power losses in the switches of the test circuit. For comparison are shown in scheme losses without "soft switching" control scheme (Fig. 6).

From fig. 5 and fig. 6 is seen that the current through transistor  $S_1$  begins to flow in the reset voltage on it. This led to a significant reduction in switching losses - in the case of pulses presented in the figure of 8730 W when dealing with

"hard switching" to 8.127 W when using "soft switching", i.e. 8722 W reduce the emitted power. Amplitude value of current through the transistor  $S_1$  at work "hard switching" is 59.37 A, when using "soft switching" is 3.15 A, i.e. with 56.22 A reducing the amplitude value.

### **IV.** CONCLUSION

A tree-phase induction motor drive fed by a PWM voltage source soft-switching QR inverter is presented. The proposed circuit uses two additional switches to create zero-voltage instants in the DC link.

The proposed drive system is modeled and its performance is simulated in PSpice. Simulation results show that the proposed scheme for the "soft switching" is obtained a significant reduction of the power losses in the power switches and the reduction of the amplitude values of the current through the transistors as compared with the scheme of "hard switching".

#### APPENDIX

Induction motor type AO-90S-4

 $P_N=1,1kW;$   $U_N=380V;$   $I_N=2,8A;$  f=50Hz;  $p_p=2;$   $n_N=1410min^{-1};$   $M_N=7,45Nm;$  cos $\phi=0,8;$   $J_m=0,001kgm^2.$  Parameters for s=s<sub>N</sub>

 $R_s$ =7.45 $\Omega$ ;  $R_r$ =5.00255 $\Omega$ ;  $L_{\sigma s}$ =0.01839H;  $L_{\sigma r}$ =0.01839H;  $L_{\sigma r}$ =0.01839H;

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