Matlab-Simulink Model of Three-Phase BUCK Rectifier with Sinusoidal PWM

Georgi Kunov and Stoyan Vuchev

Abstract – **A three-phase BUCK rectifier with sinusoidal PWM is considered in the present paper. An algorithm for control is synthesized and Matlab-Simulink model is constructed based on this algorithm. The simulation results are presented illustrating the mode of operation of the functional blocks, as well as the shape of the voltage on the load.**

Keywords – **Power Electronics, Three Phase Rectifiers, PFC Rectifiers, Sinusoidal PWM BUCK Rectifiers, Matlab-Simulink Simulation.**

I. Introduction

The rectifiers are components of many electro-technological and energetic devices. A key requirement to them is the high power factor. The first circuit solutions for improving the power factor are used in non-adjustable diode rectifiers. These are circuits of single-phase and three-phase Power Factor Correction (PFC) Rectifiers. According to the principle of operation, they are step-up (BOOST) rectifiers [1, 2].

Often it is necessary in the practice to adjust the rectified voltage from 0V to the nominal voltage. In such cases an additional step-down (BUCK) DC-DC converter is used in BOOST PFC rectifiers. This approach leads to an increase in size and to more expensive device.

The above-mentioned problem is solved by BUCK rectifiers operating under sinusoidal pulse width modulation (PWM). A review of the circuit variants of this type of rectifiers, as well as of BOOST PFC rectifiers is performed in [3, 4, 5].

In the present paper, a three-phase rectifier with sinusoidal BUCK PWM is considered and corresponding Matlab-Simulink model is synthesized. This model is valid for both active and inductive load.

II. Matlab-Simulink Model of Three-Phase BUCK Rectifier with Sinusoidal PWM

The power circuit of the Simulink simulation model of the rectifier is shown in Fig.1. It is realized by six unidirectional switches (DR1, Sw1 ÷ DR6, Sw6) and Control Unit (Subsystem CU-BUCK PWM Rectifier).

The block diagram of the Subsystems of the Control Unit is shown in Fig. 2. It, in turn, is built of of six bocks: Subsystem positive/negative High Voltage; Subsystem positive/negative Phases; Subsystem Pulse Width Modulation and three blocks with the same internal configuration - Subsystem Gate Pulses.

The purpose of each of the blocks of the Control Unit is considered separately.

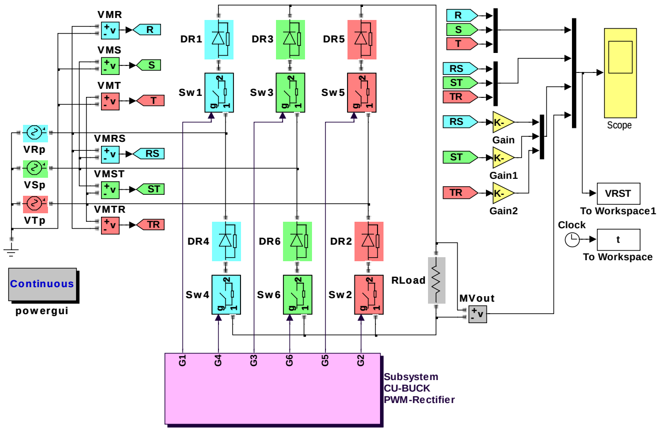

Fig. 1. Power circuit of the three-phase rectifier

A. Subsystems positive/negative High Voltage and positive/negative Phases

The circuit realizing the Subsystem positive/negative High Voltage is shown in Fig. 3. Its purpose is to produce signal "*logical* 1" for the intervals, where each of the three phases is the most positive (most negative). This is realized by three-phase diode rectifier, by controlling the current through each of the diodes.

As it is seen from the waveforms shown in Fig. 5, the phase R is most positive when the diode D1 is conducting (VCD1=1; in the interval from π/6 to π/6) and is the most negative when the diode D4 is conducting (VCD4=1; in the interval from 7π/6 to 9π/6).

The purpose of the Subsystem positive/negative Phases is to produce signal "*logical* 1" for the intervals, where each of the phases is positive (negative). Its circuit realization is shown in Fig. 4. As it is seen from the waveforms shown in Fig. 5, in the interval where phase R is positive, VRp=1 (from 0 to π) and in the interval where it is negative VRn=1 (from π to 2π)

The signals *Positive/negative High Voltage* and *positive/negative Phases* for the phases S and T are also shown in Fig. 5 and are obtained similarly.

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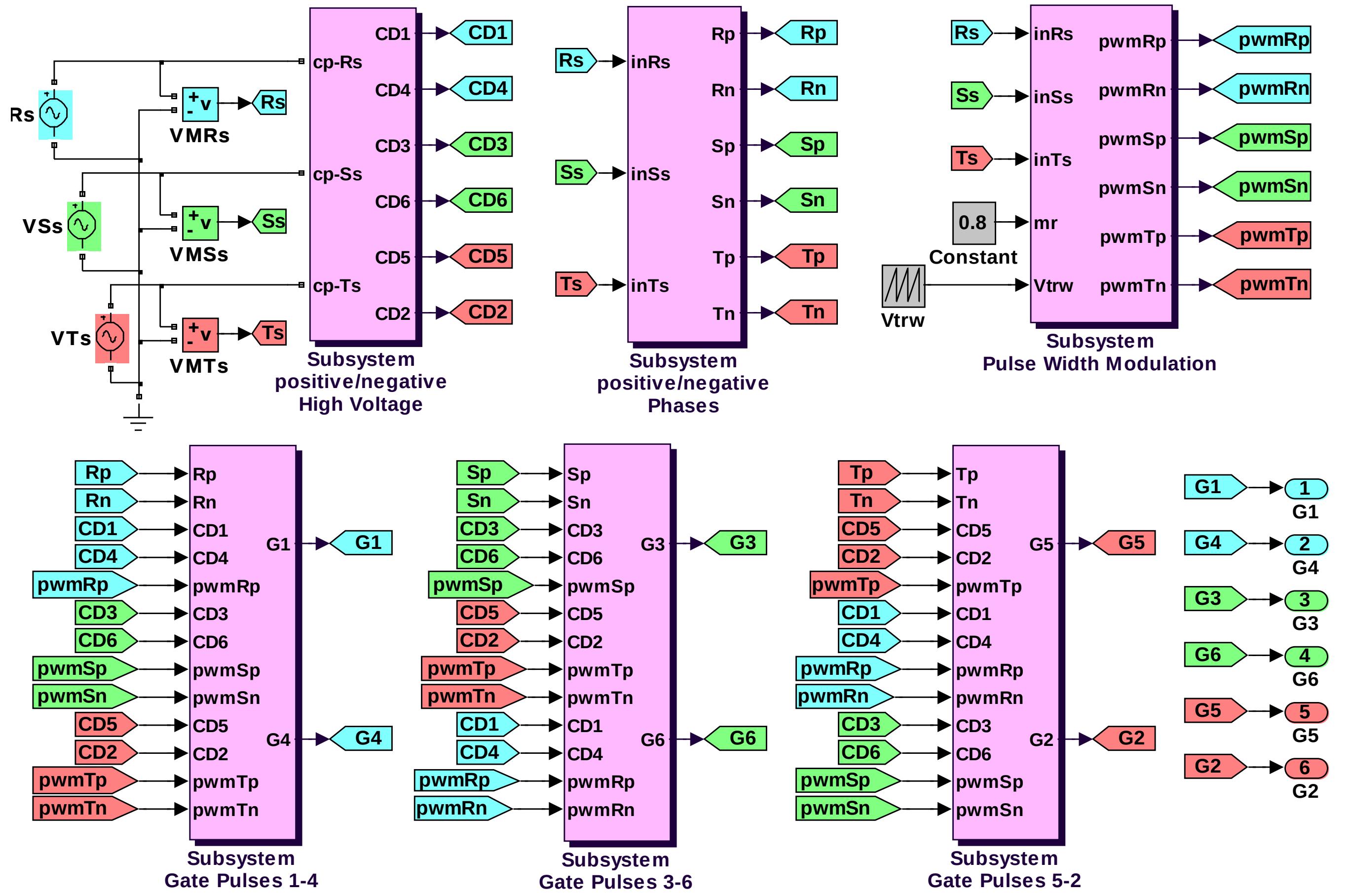

Fig. 2. Subsystems of the Control Unit

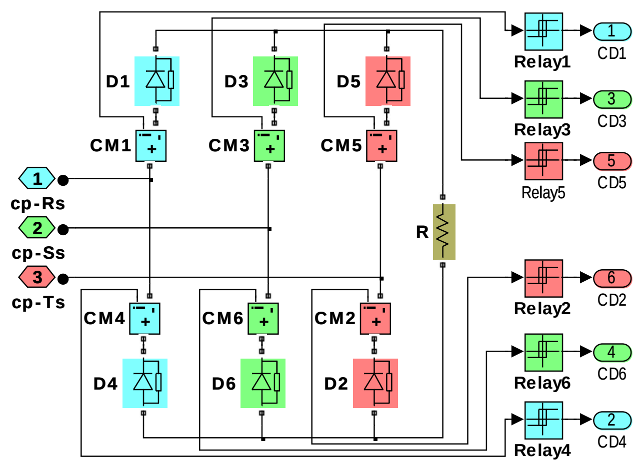

Fig. 3. Subsystem positive/negative High Voltage

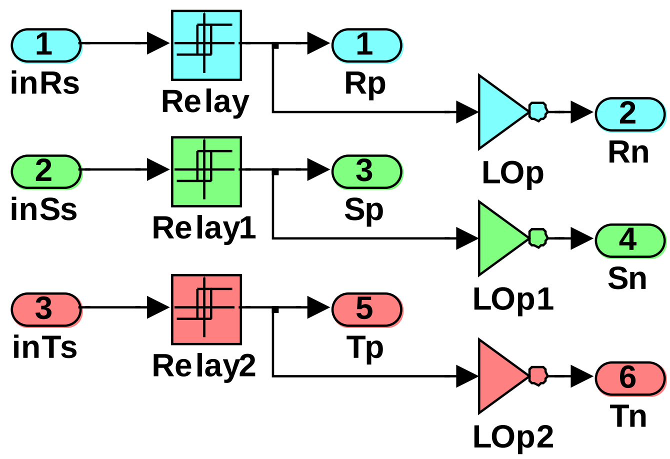

Fig. 4. Subsystem positive/negative Phases

B. Subsystem Pulse Width Modulation

The circuit realizing the Subsystem Pulse Width Modulation is shown in Fig. 6. The waveforms, illustrating its principle of operation, are shown in Fig. 7.

The sinusoidal PWM for each of the phases, is obtained by comparing the corresponding phase voltage (|VR1|; |VS1|; |VT1|) with a sawtooth voltage (Vtrw). The obtained in such a way three PWM signals (pwmRp, pwmSp and pwmTp) are supposed positive.

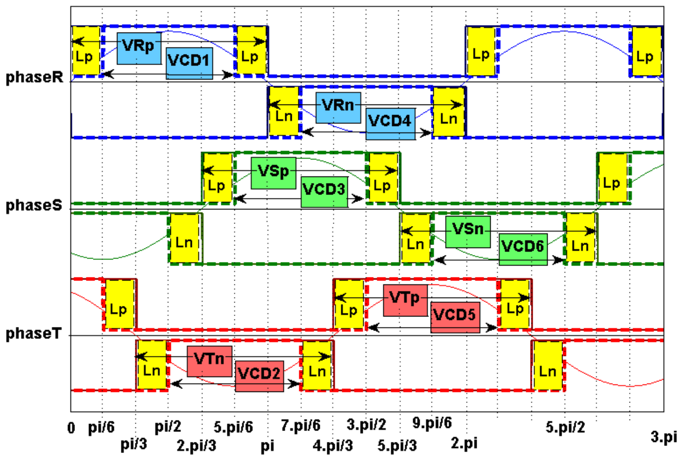

Fig. 5.Waveform of Subsystems positive/negative High Voltage and positive/negative Phases

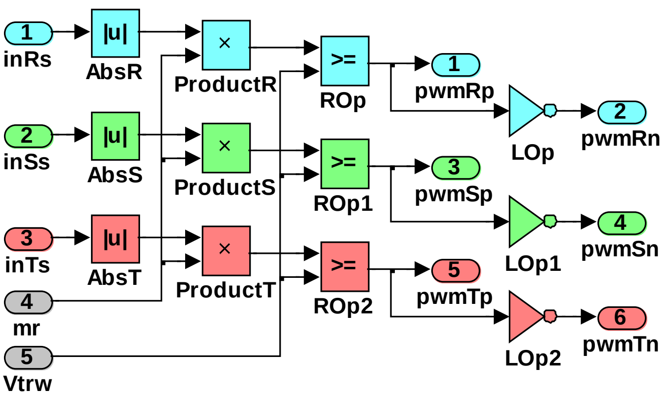

Fig. 6. Subsystem Pulse Width Modulation

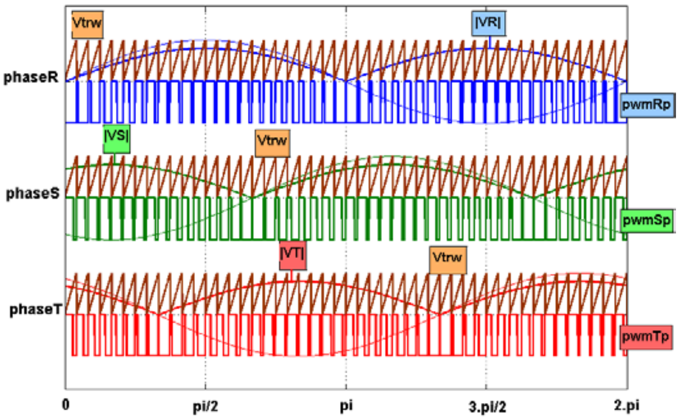

Fig. 7. Waveform of Subsystem Pulse Width Modulation

Their corresponding inverse logical values are denoted as negative values (pwmRn, pwmSn and pwmTn). Only positive PWM logical signals are presented in Fig. 7. The modulation coefficient can be varied by the signal mr ($0<m_r<1$).

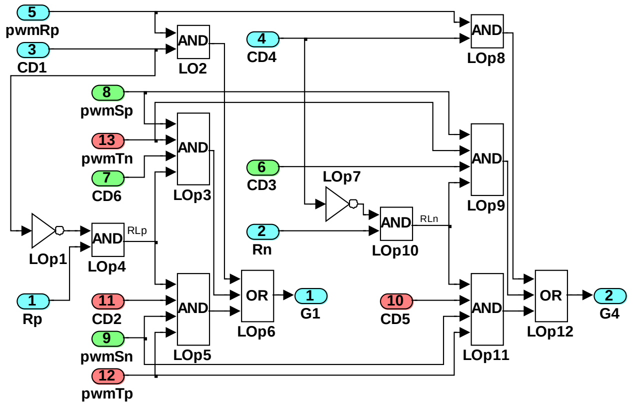

Fig. 8. Subsystem Gate Pulses 1-4

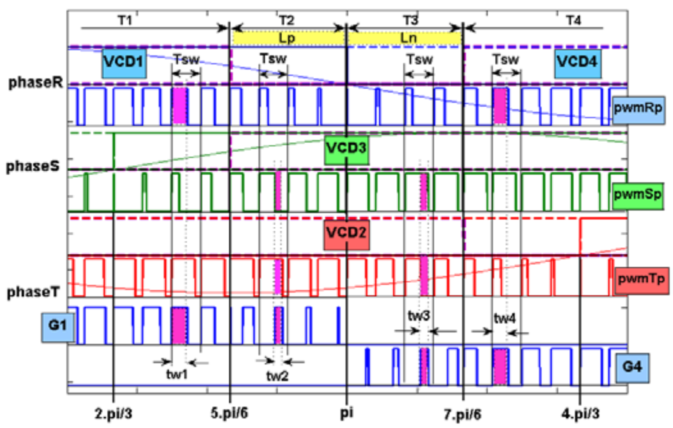

Fig. 9. Waveform of Subsystem Gate Pulses 1-4

C. Subsystem Gate Pulses 1-4

The circuit realizing the Subsystem Gate Pulses 1-4 is shown in Fig. 8. The modulated according sinusoidal law signals G1 and G4 are created using this logical circuit. The signals G1 and G4 commutate the switches Sw1 and Sw4 correspondingly (Fig.1), which are connected to power phase R (VRp).

The operation of the circuit is illustrated by the waveforms, presented in Fig. 9.

For the intervals, where the phase R is the most positive (VCD1=1; interval T1), Gate Pulses G1 coincide with those of pwmRp.

For the intervals, where the phase R is the most negative (VCD4=1; interval T4), Gate Pulses G4 also coincide with those of pwmRp.

The elements (LOp1, Lop4) and (Lop7, Lop10) realize the corresponding functions:

$$RLp=\overline{VCD1}.VRp \quad \text{and} \quad RLn=\overline{VCD4}.VRn$$

It is seen from Fig. 5, that those are the intervals where VRp=1 and VCD1=0 (denoted in Fig. 5 as Lp) and the intervals where VRn=1 and VCD4=0 (denoted in Fig. 5 as Ln).

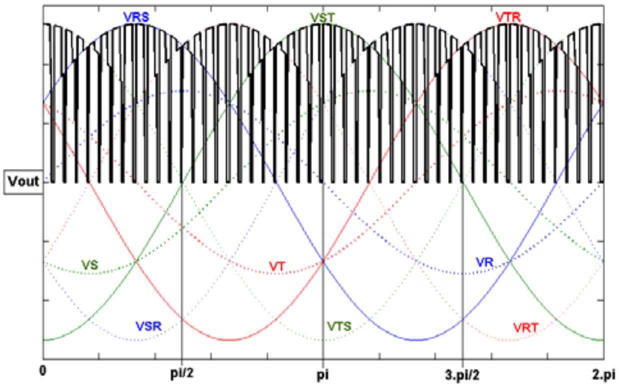

Fig. 10. Waveform of PWM output voltage

For the intervals Lp, Gate Pulses G1 are generated corresponding to the logical function:

$$G1=(pwmSp.pwmTn.VCD6 \cup pwmTp.pwmSn.VCD2).RLp \quad (1)$$

For the intervals Ln, Gate Pulses G4 are generated corresponding to the logical function:

$$G4=(pwmSp.pwmTn.VCD3 \cup pwmTp.pwmSn.VCD5).RLn \quad (2)$$

The result of the functions (1) and (2) for the intervals T2(Lp) and T3(Ln) can be seen from the waveforms, shown in Fig. 9.

The inner configuration of Subsystem Gate Pulses 3-6 and Subsystem Gate Pulses 5-2 coincides with those shown in Fig.8. The generation of Gate Pulses 3-6 and Gate Pulses 5-2 is similar to the described above, taking into account the corresponding input signals.

D. Simulation results for the output voltage

The waveform of the output voltage V_{out} on the load resistor R_{load} is shown in Fig. 10.

It is pulsing as in the three-phase bridge rectifier with a frequency 6 times higher than the mains frequency.

Due to the sinusoidal PWM, the mean value of V_{out} for each period of the modulating frequency, remains a constant value

III. Conclusion

A three-phase BUCK rectifier with sinusoidal PWM that improves the power factor has been considered in the present paper. The building blocks are described and the algorithm for control is synthesized. A Matlab-Simulink model is constructed based on this algorithm. The simulation results are given illustrating the mode of operation of the functional blocks and the waveforms of the signals are presented.

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