A Microprocessor System for Food Quality Evaluation by Hyperspectral Images

Krassimir Kolev[1]

Abstract – **The paper reports on the development of a microprocessor system base on video signal processor DM642 for food quality evaluation by hyperspectral images processing. The presented microprocessor system captures hyperspectral sliced images and makes images processing. The schematic diagram of the microprocessor system, hardware structure description, algorithm description for preprocessing by wavelet transformations and quality features reduction are given. Quality features reductions are made by extraction transformations. Experiments show that the microprocessor system has a good performance for objective quality evaluation of meat products.**

Keywords – **Microprocessor system, hyperspectral images, food quality.**

I. Introduction

Acquisition and processing of hyperspectral images is a new promising technology successfully combines the advantages of computer vision and spectroscopy methods for modern objective contactless quality food evaluation. Hyperspectral technology is a contactless nondestructive, requires no pre-treatment of samples obtained both spatial and spectral information for foods allows a more complete description of the constituent concentration and distribution in heterogeneous foods. Hyperspectral technology is very sensitive to detect small components in the samples and allows examination of foods with different geometries. Processing of hyperspectral images of food requires fast image processing hardware. Many authors report that they use hyperspectral images for food evaluation, but they have not published details of their computer systems for processing [1]. The goal of this paper to report a microprocessor system for food quality evaluation by hyperspectral images processing.

The author designs a full working microprocessor system and implements algorithms for preprocessing and features extraction for food assessment. The author uses a digital signal processor (DSP) for his proposed microprocessor system, because modern DSPs are flexible and suitable to extremely complex math intensive tasks such as hyperspectral image processing. The presented system is suitable for testing and grading for all types of food by conveyer moving. Hyperspectral scanning is not matter of this paper. Some basic algorithms are developed for system performance tests, because we know that microprocessor are useless without software.

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II. Design Diagram And Components

Considering the details of the different scanning systems for obtaining hyperspectral images is possible to synthesize modern model of computer platform for objective non-destructive quality assessment of food by processing hyperspectral images. Computer platform for determining the quality characteristics of foods consist of interconnection hardware and software components.

A model design diagram of computer platform for food quality evaluation is given in Fig.1.

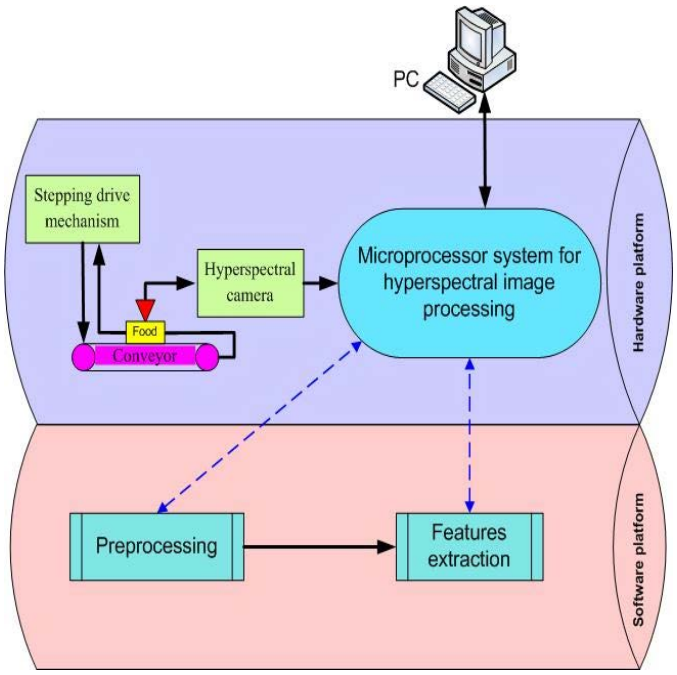

Fig.1. Design diagram of the computer platform

Presented model of the computer platform in Fig.1 shows that the hardware platform consists of stepping drive mechanism, conveyor, hyperspectral camera and microprocessor system for hyperspectral image processing. The paper highlights subsystems making hyperspectral image processing. Hardware subsystem (microprocessor system for hyperspectral image processing) consists of a high performance DSP for image processing.

Software subsystem is divided into algorithmic modules (preprocessing and features extraction) according to the tasks performed by the software associated with the preprocessing hyperspectral images and reduction of feature space.

Diagram of the hardware subsystem is shown in Figure 2.

The MT9V022 image sensor was chosen for hyperspectral camera due to its suitability for hyperspectral imaging, because it can be used in the wavelength range from 300 nm to 1100 nm of the spectrum [2]. The image sensor provides a resolution of 10 bits per pixel, is able to capture both continuous video and single frames progressively.

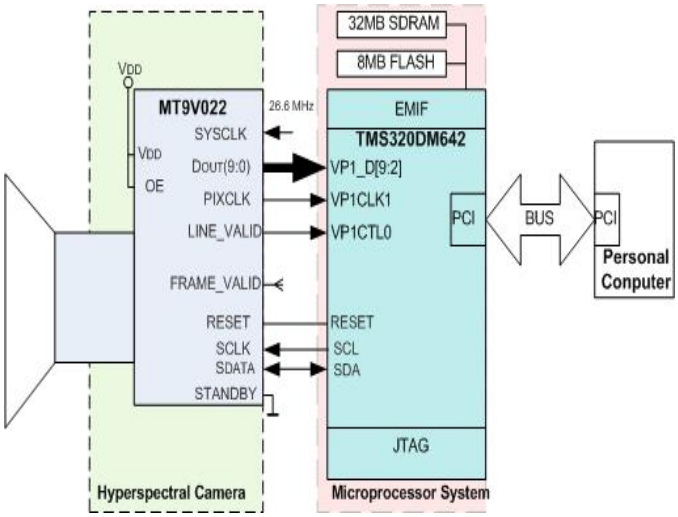

Fig. 2. Diagram of the hardware subsystem

All image sensor registers are written and read through the I^2C serial interface. The I^2C address of the MT9V022 is fixed and consists of seven bits of address and 1-bit of read/write direction. Full registers descriptions are given in datasheet of MT9V022 [2]. The image sensor interfaced to the microprocessor system through the video port of DSP TMS320DM642 (DM642). The FRAME_VALID signal on the MT9V022 is unconnected because no input exists on the DM642 which can take advantage of this signal. However, the FRAME_VALID line is not needed since the information necessary for proper operation with the DM642 is carried on the LINE_VALID signal. Recall that the LINE_VALID and FRAME_VALID signals indicate that a line and frame of valid pixel data is available on the data bus. Because the DM642 samples data when VP1CTL0 is active, proper video port and MT9V022 operation requires that the LINE_VALID signal to be connected to the VP1CTL0 signal [3].

I use the high performance DSP chip TMS320DM642 of Texas Instrument (TI) as a core, design and realize a whole hardware subsystem. The TMS320DM642 (or DM642) offers cost-effective solutions to high-performance DSP programming challenges with up to 5760 MIPS at a clock rate of 720 MHz. Its core processor has 64 general-purpose registers of 32-bit word length and eight highly independent functional units—two multipliers for a 32-bit result and six arithmetic logic units [4]. The VelociTI™ extensions in the eight functional units include new instructions to accelerate the performance in video and imaging applications and extend the parallelism of the VelociTI™ architecture. The DM642 can produce four 16-bit multiply-accumulates (MACs) per cycle for a total of 2880 million MACs per second (MMACS), or eight 8-bit MACs per cycle for a total of 5760 MMACS. The DM642 uses a two-level cache-based architecture and has a powerful and diverse set of peripherals. It also has a 64-bit seamless External Memory Interface (EMIF), which can interface to synchronous and asynchronous memories and peripherals. The TMS320DM642 DSP is IEEE-1149.1 JTAG boundary scan compatible. In order to support multimedia applications, the DM642 device has been integrated with 3 configurable Video Port (VP0, VP1, and VP2) peripherals and Multi-Channel Audio Serial Port (MCASP). The inter-integrated circuit (I^2C) module provides an interface between a DM642 and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C bus). The I^2C port on the TMS320DM642 allows the DSP to easily control peripheral devices The PCI port for the DM642 supports connection of the DSP to a PCI host via the integrated PCI master/slave bus interface. For the DM642, the PCI port interfaces to the DSP via the EDMA internal address generation hardware. This architecture allows for both PCI Master and Slave transactions, while keeping the EDMA channel resources available for other applications [5, 6].

III. Design Of The System

A. Hardware Structure

Schematic diagram of the designed microprocessor system for food quality evaluation is given in Fig.1.

The microprocessor system has a large byte addressable address space. Program code and data can be placed anywhere in the unified address space. The given system incorporates a 64 bit wide external memory interface.

Addresses are always 32-bits wide. By default, the internal memory sets at the beginning of the address space. The EMIF (External Memory Interface) has 4 separate addressable regions called chip enable spaces (CE0-CE3). The DM642 uses chip enables CE0, CE1, and CE3. The SDRAM occupies CE0 while the Flash is mapped to CE1. DM642 signals CE2 and CE3 can be use for extra components connection and expanded RAM. The microprocessor system has 32 megabyte SDRAM realized by IC7, IC8. The bus uses an external phase lock loop (PLL) device to operate the SDRAM at 133 megahertz for optimal performance. Refresh for SDRAM is handled automatically by the DM642. The PLL used for the EMIF is the IC5. The input clock to this ICS512 is 25 Megahertz via IC4. The system has 8 megabytes of Flash external memory (not shown in diagram) and connected as SDRAM to address and data bus and activates by CE1. The DM642 directly supports a PCI interface. Cross Bar Technology (CBT) mux and switches are used to separate the PCI bus from the DM642 so that the CBT's also provide +5 volt interface logic support for the PCI interface. The CBT's are automatically configured for PCI operation when the board is plugged into a PCI slot via the PCI-Detect signal. The DM642 has an internal PLL which can multiply the input clock to generate the internal clock. The PLL multiplier is set via the CLKMODE0 and CLKMODE1 pins on the DM642 device. At reset these pins are sampled, and this determines the PLL multiplier for the internal CPU clock. EEPROM IC9 connects to DM642 via I2c and it has clock generator IC10. IC6 generates reset signal for the system. .

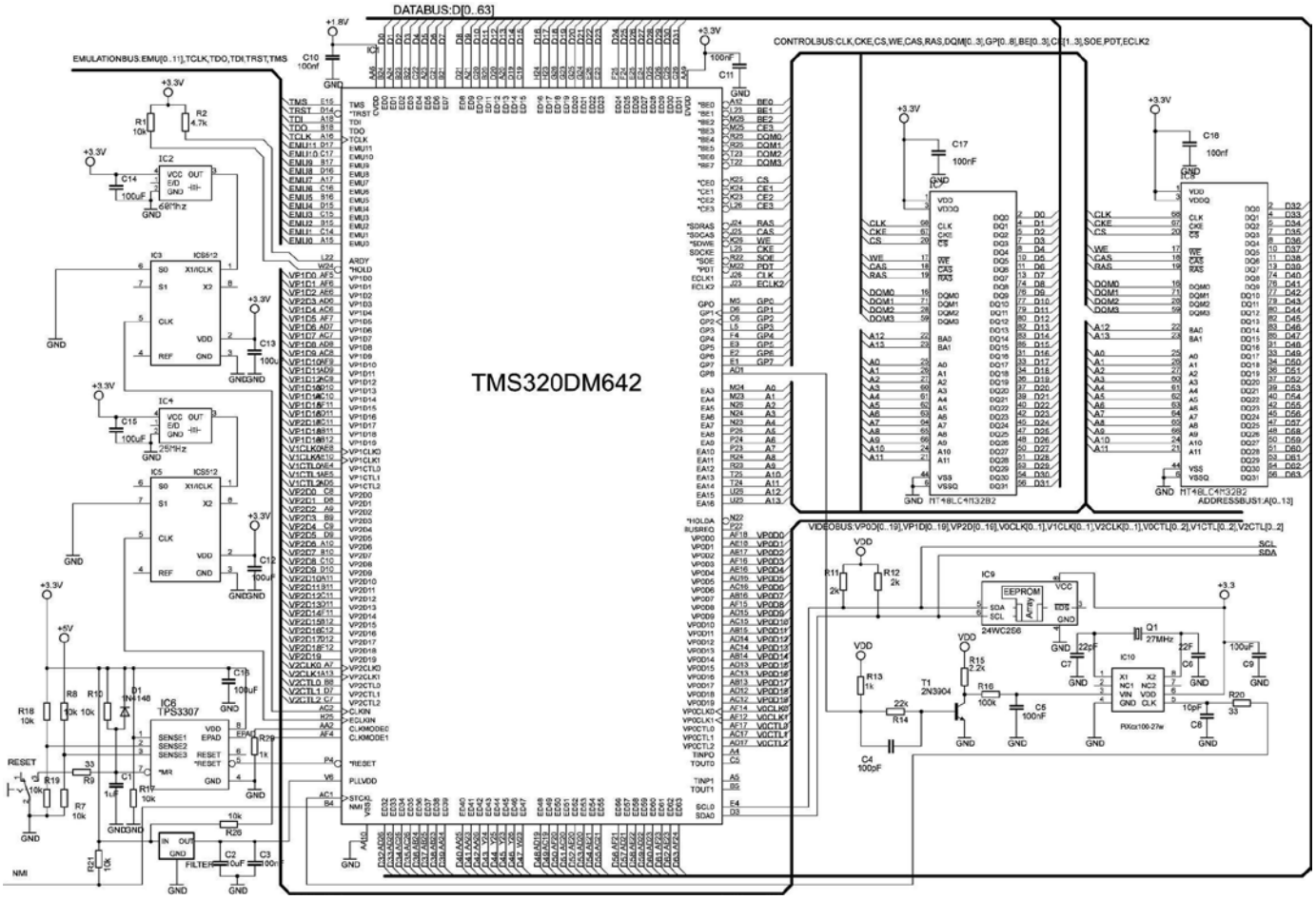

Fig. 3. Schematic diagram of the microprocessor system

B. Software Structure

Preprocessing

The hyperspectral images of food taken down in steps constitute two-dimensional images subdivided in subspaces by using multiple-resolution approximation of the initial space into low-frequency components – constituting optimum approximation and into high-frequency components constituting detailed information of the original signal [7]. The decomposition coefficients in the wavelet orthogonal basis are divided by:

$$c_{j;k,l} = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} h_{m-2k} h_{n-2l} c_{j-1;m,n} \quad (1)$$

$$d^1_{j;k,l} = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} h_{m-2k} g_{n-2l} c_{j-1;m,n} \quad (2)$$

$$d^2_{j;k,l} = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} g_{m-2k} h_{n-2l} c_{j-1;m,n} \quad (3)$$

$$d^3_{j;k,l} = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} g_{m-2k} g_{n-2l} c_{j-1;m,n} \quad (4)$$

, where c_j are approximation coefficients, d_j are the detailing coefficients.

The sequence H={h_k | k=…,-2,-1,0,1,2,…} is designated as a scaling filter.

The sequence G={g_k | k=…,-2,-1,0,1,2,…} is designated as a wavelet filter.

For Haar wavelet $h_0 = 1/\sqrt{2}$, $h_1 = 1/\sqrt{2}$, $g_0 = 1/\sqrt{2}$ and $g_1 = 1/\sqrt{2}$.

The filters divide the input signal into frequency bands. The filtered signals at the exit of the filters are obtained with double length, so after the filtration decimation is performed, i.e. removal of all odd coefficients.

The high-frequency filter (H) is related to $\psi(t)$, while the low-frequency filter (L) is related to $\phi(t)$.

The processing of images f(x,λ) with a array of dimensionality (N,M) is performed separately by rows and columns, by first performing 1-D convolution with coefficients h0(k) /low-frequency filter L/ and h1(k) /high-frequency filter H/. After that follows a decimation with a factor 2 i.e. a new array is obtained (N/2,M).

Upon processing by columns also 1-D convolution h0(k) /low-frequency filter L/ is applied and h1(k) /high-frequency filter H/ and then decimation with a factor 2.

Thus a single high-scale approximation is performed. As approximating coefficients C_1 are in a matrix form with dimensionality (N/2), M/2). It is possible to apply for a second time high-scale approximation on the matrix with approximation coefficients whereby a new reduction of the feature space is obtained up to approximation coefficients C_2. This process of dual-scale approximation has been illustrated in Figure 4.

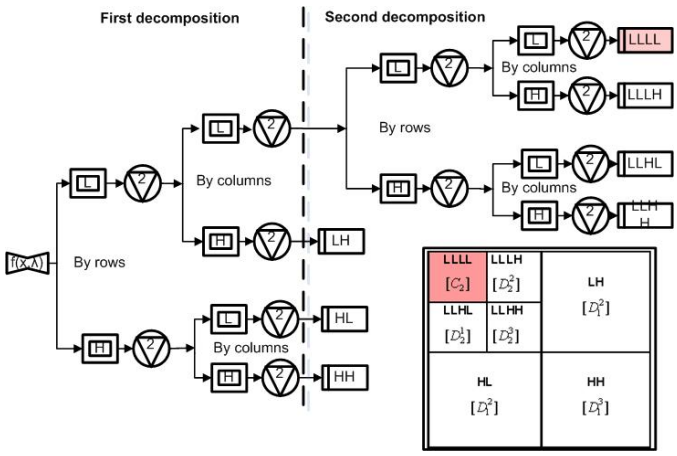

Fig. 4. Diagram of two levels transform of sliced hyperspectral image

Feature Extraction by Independent Component Analysis (ICA)

To estimate n independent components, the algorithm is run for n times. The steps of Fast-ICA for separating an independent component are shown.

1. Pre-whiten the observed image data to obtain a whitened signal v.

2. Take a random initial vector $w(0)$ and normalize it to unity, i.e., $w(0) = w(0)/\|w\|^2$, and set j = 1.

3. Set $w(j) = E\{v(w(j-1)^2 v)^2\} - 3w(j-1)$. The expectation operator can be estimated using a large number of samples.

4. Set $w(j) = w(j)/\|w(j)\|^2$ i.e., normalize $w(j)$.

5. If $|w^T(j)w(j-1)|$ is not close to 1, then set j= j+1 and repeat step 3. Otherwise output vector $w(j)$.

6. Using $w(j)$, one of the separated signals is given by

$$s(k) = w^T(j)v(k), \quad k = 1,2,...$$

An orthogonalizing projection has to be added inside the recursive loop of this algorithm to estimate different components each time.

C. Testing of the System

The development test of the proposed microprocessor system was made by JTAG emulator XDS560 connected between DM642 and personal computer ASUS M51AC i7.

The performance of data processing is tested in real-time. The connection of Video Port 1 to hyperspectral camera is similar to the way described in this paper. The data for test is 320x240x16bits video stream from hyperspectral camera CCD sensor. In the experiment 24 linearly scanned hyperspectral images were used of ready-to-cook minced meat products. The algorithms are realized in C program environment for digital signal processor DM642 of Texas Instruments. The analysis of the video signal is line oriented. Table 1 shows the results obtained per time for machine processing for one step of scanning /one slice/ for each of the algorithms realized upon fixed eight features of reduction.

TABLE 1
VALUES OF PROCESSING TIME IN HARDWARE IMPLEMENTATION

Algorithms	Machines cycles	Processing Time Value [s]
Initialization	2125	$1.53*10^{-06}$
Preprocessing (dual-scale Wavelet)	169444444	0.061
Features Extraction	6337722222	2.28158
Total:	6507168791	2.34258

The actual power consumption in this experiment with proposed microprocessor system based on DM642 is 6.47 W. The total maximum power consumption of all components of the microprocessor system is less than 9 W, according to component manufacturers.

IV. CONCLUSION

The performance test result shows that this microprocessor system has total processing time under 120 seconds per 50 slides quality tracking. This system could be applied to build computer platform for fast objective quality food evaluation by hyperspectral image processing. The proposed microprocessor system based on high performance video signal processor DM642 has small size and can use as mobile quality evaluation platform on production lines and shops.

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