An Experimental Setup for Switching Noise Measurement in Monolithic On-Chip Antennas

Hristomir Yordanov[1]

Abstract— **On-chip integrated antennas are of growing interest for the development of miniaturized sensors, as they allow for a reduction of the cost and dimensions of the autonomous systems. The amount of chip area dedicated to the antenna should be minimal. One way to achieve that is to share available chip metallisation, such as the ground supply plane, between the antenna and the on-chip digital circuitry. This can lead to interference between the circuit and the antenna. This paper presents an experimental setup for the measurement of this interference and for evaluation of the possible degradation of a wireless link between on-chip integrated antennas.**

Keywords— **Embedded antennas, Noise measurement, On-chip integrated systems.**

I. Introduction

The on-chip integrated antennas are an interesting alternative to wired chip-to-chip communications. They can provide high data rates, reduce system development time, and allow for system miniaturization, which is of great interest for the development of miniaturised sensors and sensor systems. Integrated antennas can be manufactured using standard or modified CMOS technology, where the modifications are in order to reduce the RF losses in the substrate [1], [2]. The CMOS technology allows for development of RF front end circuitry up to the millimetre wave band [3]. Therefore we can fabricate a single chip device, capable of acquisition, processing and wireless transmission of data.

The antenna integration should be chip area efficient in order to reduce the manufacturing costs. This can be achieved by sharing available CMOS metallisation between the digital circuitry and the antenna. For instance the CMOS ground plane could be shaped such that it also supports antenna mode currents [4]. This is a potential source for interference between the antenna and the digital circuitry. The interference goes both ways: the antenna currents can lead to an increased bit error rate of the digital circuit, and the transistor switching noises can induce RF power at the antenna terminals. In order to reduce the interference effects, the antenna operating frequency is designed in the millimetre wave range, well above the typical clock frequencies of the digital circuits. In this case the effect of the antenna currents on the digital transistors can be neglected due to their low-pass nature. This assumption has been experimentally proven by Bohorquez and O [5]. This paper is a step towards the experimental proof of the opposite effect. It provides a way to measure the RF power induced on the antenna terminals due to the switching currents of digital MOS transistors.

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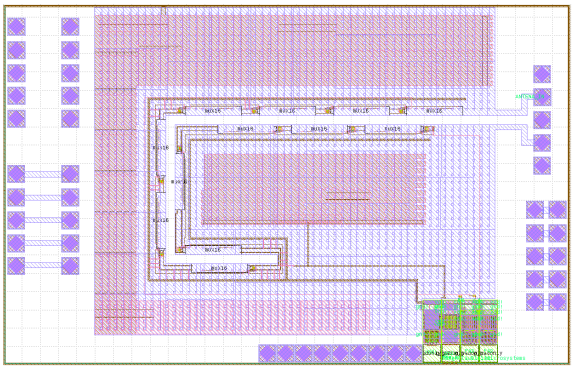

Fig. 1. Layout of the designed chip

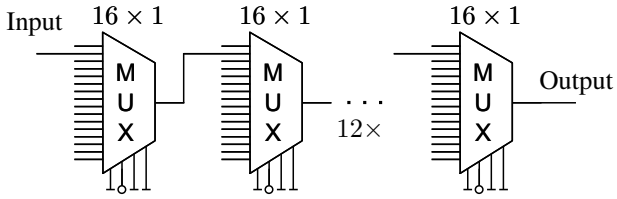

Fig. 2. A schematic of the implemented digital circuit. It consists of 12 multiplexors, hard-wired so that the input signal propagates to the output.

II. Experimental Chip Description

The layout of the experimental integrated circuit is presented in Fig. 1. It consist of a L-shaped slot antenna, open-circuited at the port side, operating at 24 GHz. We have selected this frequency due to the limitations of the available 0.35 μm CMOS technology, which does not allow transistor switching faster that 500 MHz. Therefore, in order to estimate the induced noise in a 60 GHz antenna due to a 1.3 GHz clock, we have designed a scaled prototype with the same ratio of clock to carrier frequency.

Full-wave electromagnetic models of the antenna show that the current density is highest along the antenna edges. This means that transistor switching currents generated in this area are expected to induce greatest RF power at the antenna terminals. Therefore the digital circuits which generate the interference are located only along the antenna edge. The circuitry consists of twelve 16-to-1 multiplexors, connected in series, as shown in Fig. 2. They are hard wired so that the input signal propagates through all of them and is routed to the output. The multiplexers consist of 270 transistors each. In the described configuration 32 transistors switch state and therefore draw current every time the input signal switches from high to low or from low to high, which is a representative

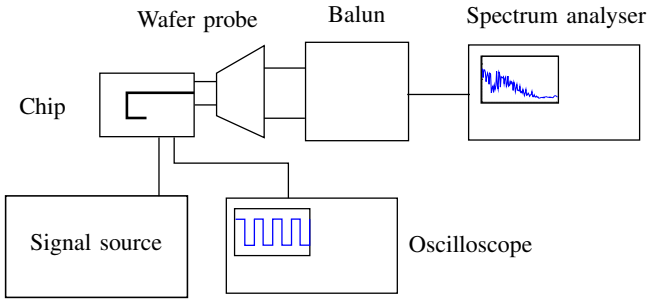

Fig. 3. Measurement setup for direct noise power measurement.

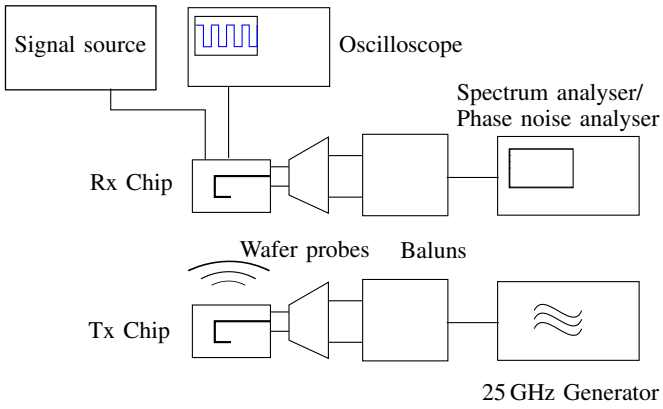

Fig. 4. Measurement setup for direct noise power measurement.

transistor usage efficiency for a typical digital circuit. The excitation is a series of alternating '1's and '0's with variable data rate. It is fed from the input pin to the upper-right multiplexer above the slot in Fig. 1, propagates through the rest 11 of them and exits from upper-right one below the slot, and is routed to the output pin below. The propagating signal is digital, with frequency up to 500 MHz.

The layout contains TLR calibration structures for measuring the antenna input impedance, which is required for noise power measurement calibration. The chip has 4 connected low-frequency pins, located on the bottom side, which are for Vcc, GND, Input and Output, and five RF pins on the right hand side, connected to the antenna.

III. Measurement Setup

Two approaches for measuring the noise power are possible with the designed chip. First is the direct approach by connecting a spectrum analyser directly to the antenna port. This setup is presented in Fig. 3. The chip will be measured using a wafer probe, without bonding or housing. The signal source provides rectangular pulses with V_{ss} amplitude and variable frequency in the range 30 – 100 MHz. The functionality of the digital part of the integrated circuit will be verified by monitoring the output using an oscilloscope. The on-chip antenna is connected to a spectrum analyser via a GSGSG wafer probe and a balun, coupling the symmetric antenna port to the unbalanced spectrum analyzer port. The balun has been realized using an in-house developed rat-race coupler.

The second approach is to use two on-chip antennas and transmit a CW signal over the link. We were looking for changes of the input level and of the phase noise at the receiver side. The setup is presented in Fig. 4. We can also use this setup to evaluate the insertion loss of the channel and thus estimate the antenna gain and efficiency.

IV. Expected Results

The switching current due to the digital transistors is periodic, because the input signal, fed to the multiplexers is also periodic. Therefore it can be expected, that the induced RF power on the antenna terminals will have its peak power at frequencies close to the frequency of the digital signal. On the other hand, the length of the antenna is comparable to the wavelength of the wireless signal. This suggests that the currents due to each transistor along the antenna edge should be seen from the antenna terminal with a different phase. This suggests that we can expect a $1/f$ type of noise, which typically arises in similar scenarios. The experiment should confirm the assumption for $1/f$ noise and give an estimate on its rate of decay in frequency.

Additional information that can be obtained from the experiment is the evaluation of the antenna efficiency. It is expected to be low, because the standard CMOS substrate has very high losses in the RF frequency ranges, and no measures could be taken to reduce that losses, as standard CMOS technique is used for the chip manufacture. Furthermore, the insertion loss of a link between two antennas can be measured and an estimation of the capacity of such a link can be made.

V. Summary

This paper presents an experimental set-up for measurement of the noise, induced in an on-chip integrated antenna due to the switching currents of the digital transistors, available on the same chip. The problem arises due to the high space coupling of the antenna and the digital circuitry, arising from the fact that the antenna uses the CMOS ground supply plane metallisation. The experimental chip is described, along with the proposed measurement setup, and the expected results have been described.

Acknowledgement

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