# Hysteresis Controlled Switching-Mode Amplifier for LTE Applications

Tihomir Brusev

*Abstract* – **Switching-mode amplifiers are used in power supply circuits, which deliver the energy to the transmitter's power amplifier (PA) for fourth generation Long-Term Evolution (4G LTE) applications. They could be part of series or parallel hybrid envelope amplifier (EA) architectures in combination respectively with linear amplifier. In this case switching-mode amplifier supplies about 80% of necessary power to the PA. Therefore efficiency of this stage strongly affects the overall efficiency of the envelope tracking power amplifier (ET PA) system. Switching-mode converters are used also in the interleaved multiphase structures, which perform the function of EA in 4G LTE transmitter. In this paper are presented investigation results of hysteresis controlled switching-mode buck converter designed on CMOS 0.35 µm process.**

*Keywords* – **switching-mode converter, CMOS 0.35 µm process, Cadence, LTE wireless communication standard.**

## I. INTRODUCTION

In the new wireless communications 4G LTE standard high data rate can be transferred [1], [2], [3]. This gives freedom to the costumers to watch TV programs in their mobile phones, to have fast web browsing, etc. All those advantages compare to the GSM communication standard are connected to a drawback that the battery has to be recharged more often. Efficiency improvement of the separate building blocks in the transmitter is the key to save batteries energy of the mobile communication devices.

Increasing the system run-time of battery powered portable electronic devices is challenging task. Stringent linearity requirements for PA, which is the most energy consuming block in the transmitter, should be fulfilled. On the other hand linear PAs are not high efficient circuits. Their efficiency is unacceptable small especially when they work with low power input signal. PA of the transmitter in LTE applications have to work with high peak to average power ratio (PAPR), which lead to decreasing of efficiency values of this stage [4]. In most of the time PA have to work in the back-off mode of operation.

Envelope elimination and restoration (EER) and envelope tracking (ET) are efficiency enchantment techniques for PA [4], [5]. The both method used modulated supply voltages which are delivered to the RF PAs transistor. ET has some advantages compare to EER technique, such as lower bandwidth required to envelope amplifier and higher output gain at low power of PA [4], [6]. Those features help higher power-added-efficiency (PAE) of the whole system to be achieved when ET technique is used.

Envelope amplifier in ET technique is used to supply dynamically changeable voltages to the drain or collector of PA's output transistors as a function of PA input signals. The main goal is RF PA's transistor to operate near to saturation mode in most of the working time [7]. Overall efficiency of the ET PA system is defined by formula [8] (1):

$$\eta_{ET\,PA} = \eta_{EA}.\eta_{PA}, \quad (1)$$

where $\eta_{EA}$ is the efficiency of the envelope amplifier; $\eta_{PA}$ is respectively the efficiency of the PA.

Hybrid combination of parallel or series connected linear and switching amplifier are usually used for envelope amplifiers architectures. The function of switching amplifier is performed by switching-mode dc-dc converter. This stage delivers about 80% of the total output to the PA [6]. In some applications interleaved multiphase switching-mode buck dc-dc converters are used as envelope amplifiers [1]. The common thing in the all architectures of EAs is that switching-mode converters play a major role in determining the overall efficiency of the ET PA system.

In Section II are discussed different power supply circuit architectures for mobile communication applications, where switching-mode converters are used. Hysteresis controlled switching-mode amplifier is designed with Cadence on CMOS 0.35 µm process. Power losses in output MOS transistors are considered and evaluated. Efficiency of the whole converter system as function of load is investigated. The received results are presented in Section III.

## II. SWITCHING-MODE CONVERTER ARCHITECTURES USED IN POWER SUPPLY CIRCUITS FOR COMMUNICATION APPLICATIONS

### *A. PWM controlled buck dc-dc converter*

In the earlier communication standards like GSM, PWM controlled switching-mode dc-dc converters are used to deliver supply voltage to the PA of transmitter. These types of circuits are suitable for constant envelope signals, when stable dc output voltage of the converter should be ensured. In the 4G LTE standard envelope amplifiers, which have to supply voltage to the PA, should have fast tracking speed because envelope frequency is increased. The disadvantage of the PWM controlled switching converters is that they are low bandwidth circuits. The switching frequency $f_s$ of the dc-dc converter have to be about ten times higher than the bandwidth of the LTE signal [1]. In Fig. 1 is shown block

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diagram of switching-mode buck dc-dc converter system with Pulse-Width Modulation (PWM) control.

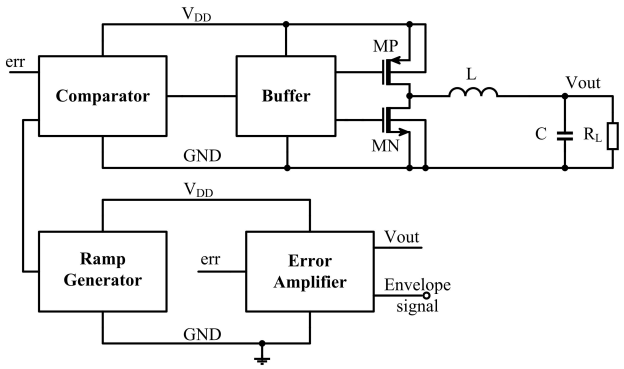


Fig. 1. Switching-mode buck dc-dc converter with PWM control system.

If PWM controlled switching-mode regulator is used as envelope amplifier in the transmitter, $f_s$ have to be very high in order to be covered all the LTE bandwidths. Power losses in the dc-dc converter will be increased, because they are proportional to the $f_s$, decreasing overall efficiency in the system.

*B. Hybrid envelope amplifier architectures*

Hybrid combination between switching-mode converter and linear amplifier is an alternative for envelope amplifier architectures [2]. Switching-mode amplifier is used to deliver low frequency and dc voltages, while linear amplifier has to supply high frequency voltages to PA. In Fig. 2 is shown series combined hybrid architecture between switching-mode buck dc-dc converter and linear amplifier [9].

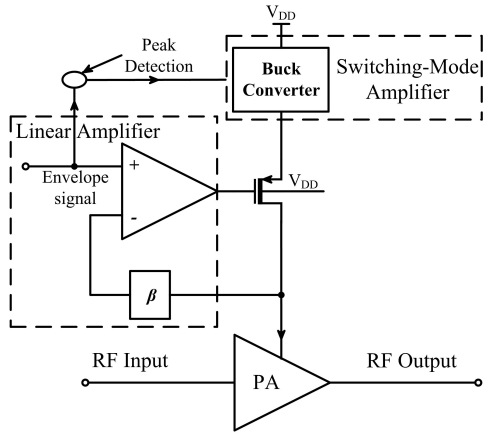


Fig. 2. Series combined switching and linear regulator topology of envelope amplifier.

In the LTE communication standard the transmitted signals have non-constant envelope waveform. Any noises coming from envelope amplifiers will be mixed and amplified with the input signal of PA, distorting output transmitted signal. Linear amplifier in the hybrid architectures should act as filter for output ripples generated from buck dc-dc converter. The disadvantage is that for high switching frequency $f_s$ linear amplifier has low power supply rejection ratio (PSRR) [2]. Also, the entire power deliver to the PA goes through power MOS transistor of the switching-mode amplifier. Therefore switching power losses will be increased especially for high $f_s$.

In Fig. 3 is illustrated block circuit of parallel combined hybrid architecture between switching-mode buck dc-dc converter and linear amplifier.

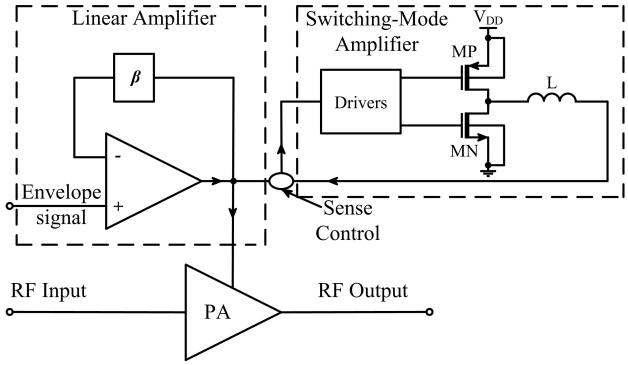


Fig. 3. Parallel combined switching and linear regulator topology of envelope amplifier.

This structures use the advantages of the both stages: high efficiency of the switching-mode converter at low frequency and wideband performance of linear amplifier. The switching-mode amplifier is used to deliver average power to PA. Linear amplifier has to filter the current ripples generated from switching type of converter and also to deliver the rest part of the power to PA, when switching regulator cannot respond quickly. The disadvantage of linear amplifier is that those circuits have low efficiency especially in the case when difference between output and input voltage is big. The parallel combined hybrid envelope amplifier architecture is widespread used for envelope amplifiers in LTE applications, because most of the envelope powers have low frequency [2], [4]. In this case high efficient switching-mode amplifier delivers most of the energy to PA, increasing overall efficiency of the system.

*C. Multiphase switching-mode amplifier architectures*

Multiphase envelope amplifier architecture is proposed in [1]. In this power supply circuit's topology less efficient linear stage is completely removed. Therefore overall efficiency of the envelope amplifier could be increased. The authors proposed interleaved two-phase switching converter architecture. In Fig. 4 is shown first stage of the proposed synchronized adaptive voltage tracking (SAVT) controller of the interleaved buck converter.

The second stage is phase shifted on 180°. The first advantage of the multiphase structures is that current and voltage ripples are decreased compare to standard buck converter.

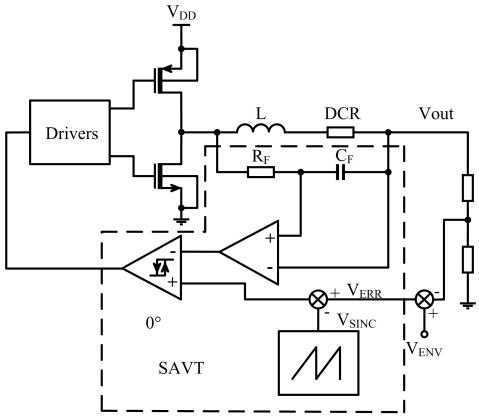


Fig. 4. Synchronized Adaptive Voltage Tracking (SAVT) control of the two-phased interleaved .converter proposed in [1].

The switching frequency $f_s$ and the phase of the two sub-converters are synchronized in the implemented hysteresis control. Thus the spectrum of the inevitable switching noises going to power amplifier could be predicted.

## III. INVESTIGATION OF HYSTERESIS CONTROLLED SWITCHING-MODE AMPLIFIER

The most used envelope amplifiers architectures for LTE applications reported in the literature and drawbacks of PWM controlled switching-mode converters have been discussed in the previous section of this paper. In the hybrid envelope amplifiers hysteresis control is used for switching-mode amplifier. This control method allows increasing of switching converter's bandwidth up to switching frequency $f_s$ [1]. Therefore using lower $f_s$, compare to the PWM control technique, the LTE bandwidths could be covered.

The hysteresis controlled switching-mode amplifier is designed on CMOS 0.35 µm process. The block diagram is presented on Fig. 5.

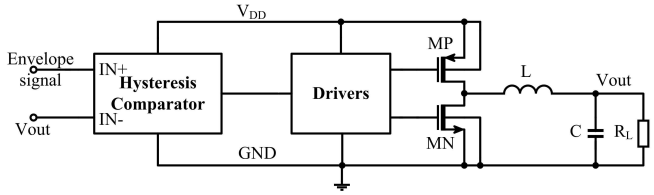


Fig. 5. Hysteresis controlled switching-mode amplifier.

Supply voltage $V_{DD}$ of the hysteresis controlled switching-mode amplifier is chosen to be equal to 3.6 V, which a standard output voltage of lithium-ion battery. The value of the inductance of output filter inductor $L$ is equal to 250 nH. The value of the capacitance of the output filter capacitor $C$ is set to be 5 pF. This is equivalent value of the capacitance of parallel combination of the power transistor of linear amplifier and the filter inductor $L$ of the parallel combined hybrid envelope amplifier architecture [6].

In Fig. 6 is presented the circuit of the comparator with hysteresis used in the investigated control. The generated output signal of this stage is applied to the drivers, which regulate the output transistors of the switching converter. The drivers provide short gap time when NMOS and PMOS transistors are both switched-off, preventing the short-circuit losses.

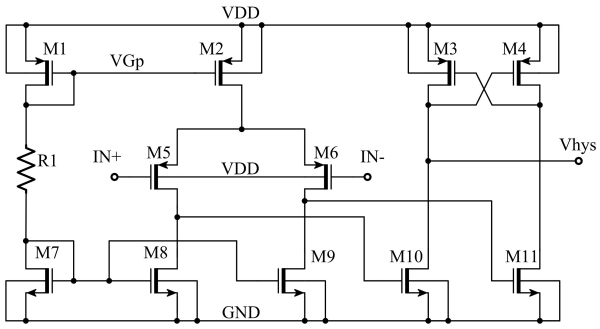


Fig. 6. Comparator with hysteresis.

The main focus of the investigation of the hysteresis controlled switching-mode amplifier is power losses in the output transistors MP and MN. They consume most of the energy of the converter determining to large extent efficiency his efficiency. Power losses in the MOS transistors are equal to [10]:

$$P_{loss,MOS} = P_{cond} + P_{sw}, \quad (2)$$

where $P_{cond}$ and $P_{sw}$ are respectively conduction and switching losses in the output transistors. On the other hand $P_{cond}$ are given by [10]:

$$P_{cond} = I_{source}^{\ 2} . r_{on,p} + I_{sink}^{\ 2} . r_{on,n}, \quad (3)$$

where $I_{source}$ and $I_{sink}$ are respectively sourcing and sinking current of the MOS transistor, while $r_{on,p}$ and $r_{on,n}$ are on-resistance of PMOS and NMOS transistors. The switching losses are equal to [2]:

$$P_{sw} = f_s . C_{tot} . V_{DD}^{\ 2}, \quad (4)$$

where $C_{tot}$ is the input total capacitance of the MOS transistor.

Power losses in PMOS and NMOS transistors of the designed converter are investigated as a function of the load $R_L$. The received simulation results are given in Table I.

The values of resistor $R_L$ represent the current load of RF PA. The reported simulation results are received when the envelope input signal of comparator with hysteresis has a sinusoidal waveform. The frequency of this test signal is equal to 20 MHz. Thus fast changing LTE envelope could be emulated. The dc voltage level of the test signal is equal to 1.5 V, while the amplitude is 250 mV. The main goal of this analysis is to be illustrated the function of losses in the output transistors of hysteresis controlled switching-mode amplifier when output power is changed.

TABLE I
POWER LOSSES (OF PMOS AND NMOS TRANSISTORS) AND EFFICIENCY AS A FUNCTION OF LOAD RL

| | $R_L$=10 [Ω] | $R_L$=15 [Ω] | $R_L$=20 [Ω] | $R_L$=25 [Ω] | R=30 [Ω] |
|---|---|---|---|---|---|
| $P_{out}$ [mW] | 83.6 | 95.35 | 113.1 | 144.2 | 217.3 |
| $P_{NMOS}$ [mW] | 1.88 | 2.12 | 2.67 | 4 | 5.834 |
| $P_{PMOS}$ [mW] | 38.23 | 45.24 | 58.7 | 90.44 | 198.3 |
| Eff. [%] | 50.34 | 58.04 | 62.06 | 63.86 | 64.58 |

In Fig. 7 are presented graphically power losses of PMOS and NMOS transistors as function of output power of the switching-mode amplifier.

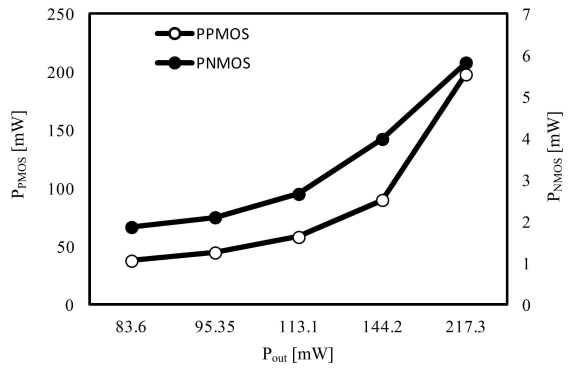


Fig. 7. Power losses of PMOS and NMOS transistors as function of output power of the switching-mode amplifier.

Simulated efficiency results of the switching-mode amplifier as a function of the load $R_L$ are presented in Fig. 8.

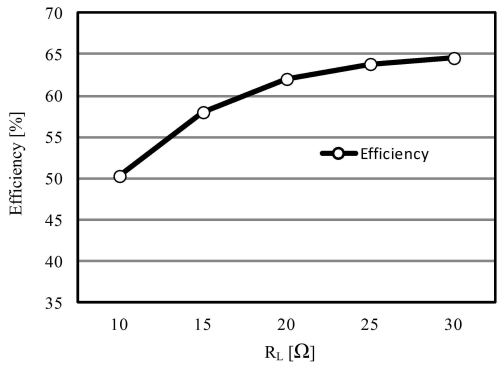


Fig. 8. Efficiency of the switching-mode amplifier as a function of the load $R_L$.

The values of the $R_L$ are changed in the range between 10 Ω and 30 Ω. This range represents practical equivalent value of PA used as a load [10]. The maximum simulated efficiency of the hysteresis controlled switching-mode amplifier is 76.7 % at output power equal to 260 mW.

## IV. CONCLUSION

In this paper are discussed different power supply circuit architectures suitable for portable communication devices, where switching-mode converters are used. The advantages of hysteresis instead of PWM control technique for LTE applications are considered. The output transistor's power losses of the hysteresis controlled switching-mode amplifier, designed on CMOS 0.35 µm process, are analyzed. Efficiency of the whole converter system as a function of the load is investigated.

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