Analysis and Design of a Resonant Reset GaN Forward Converter with Self-Driven Synchronous Rectifiers

Zoran Zivanovic[1] , Vladimir Smiljakovic[2] and Sinisa Jovanovic[3]

Abstract – **This paper presents the straightforward design of a resonant reset forward converter using a Gallium Nitride transistor with synchronous rectification. The prototype has been built and tested through lab measurements to verify the design. Design steps are described and well documented with measurement results.**

Keywords – **Efficiency, forward converter, GaN, resonant, self-driven, synchronous rectifier.**

I. INTRODUCTION

A forward converter is a popular choice for low output voltage DC/DC converters, particularly for input voltage range of 18 to 36V or 36 to 72V. It has a single primary side switch and after each switching duty cycle, the magnetizing current in the transformer has to be reset to prevent core saturation. The active clamp approach is far the best in terms of optimal performance but not so simple. Traditional reset circuits are Third Winding, RCD Clamp, Zener Clamp, Active Clamp and Resonant Reset. As the output voltage is decreased, the efficiency of the forward converter becomes limited by the output rectifier loss. Although the Schottky diodes are widely used, synchronous rectification is needed to realize higher efficiency.

II. ABOUT THE CHOSEN TOPOLOGY

The chosen topology is the forward converter with resonant reset shown in Fig. 1. This converter differs from a basic design in three ways: it uses a resonant reset technique to reset the transformer, uses Gallium Nitride transistor Q instead a MOSFET and employs synchronous rectifiers Q_1 and Q_2 (low R_{dson} MOSFETS) on the secondary side. To keep the circuit simple and low cost, the synchronous rectifiers are self-driven, directly with the voltage from the transformer secondary. The drain of Q_1 is connected to the gate Q_2, and the drain of Q_2 is connected to the gate of Q_1. The gate-drive voltages must be high enough to ensure low FET resistance, but small enough to prevent the gate destruction. The gate-drive voltage for rectifier Q_2 is derived from the reset voltage so the resonant reset is not the most efficient solution especially at high input voltage when the dwell time is large. During the dwell time the body diodes of Q_1 and Q_2 with

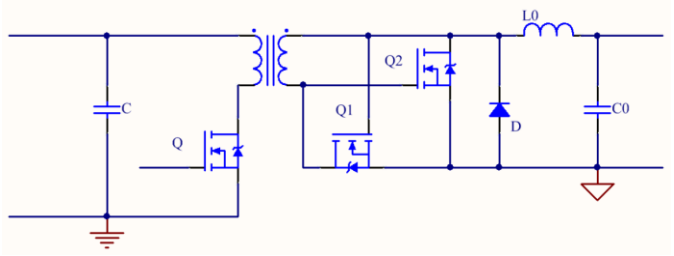

Fig. 1. Resonant reset forward converter

relatively high voltage drops are conducting and the efficiency is reduced. This loss is minimized by connecting Schottky diode D in parallel with mosfet Q_2.

The resonant circuit consists of only parasitic elements and there is no need for additional external components. When the primary switch is turned off, a resonance is developed between magnetizing inductance of the transformer and the equivalent resonant capacitance of the circuit. The high voltage across the drain of the switch resets the transformer core. There is no need for a reset winding and diode.

Typical drain voltage of primary switch in resonant reset forward converter is given in Fig. 2.

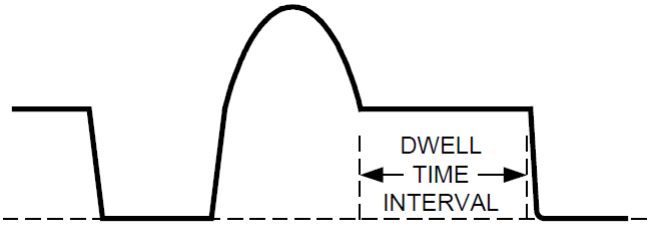

Fig. 2. Resonant reset waveform

Resonant frequency is given by

$$f_{RES} = \frac{1}{2\pi\sqrt{L_M C_R}} \tag{1}$$

where L_M is transformer primary magnetizing inductance and C_R is parasitic capacitance.

On the other hand the resonant half-sine wave voltage has a peak value given by

$$V_{RESET} = \frac{V_{INMIN} D_{MAX}}{L_M f_{SW}} \sqrt{\frac{L_M}{C_R}} \tag{2}$$

The construction of the GaN transistor allows for inherent high speed operation so the switching time of 5 ns or less are possible. The GaN transistor is not avalanche rated at the breakdown of drain-source junction so it is necessary to insure

[1]Zoran Zivanovic is with the IMTEL KOMUNIKACIJE AD, Bul. Mihajla Pupina165b, 11070 Belgrade, Serbia, E-mail: zoki@insimtel.com.

[2]Vladimir Smiljakovic is with the IMTEL KOMUNIKACIJE AD, Bul. Mihajla Pupina165b, 11070 Belgrade, Serbia, E-mail: smiljac@insimtel.com.

[3]Sinisa Jovanovic is with the IMTEL KOMUNIKACIJE AD, Bul. Mihajla Pupina165b, 11070 Belgrade, Serbia, E-mail: siki@insimtel.com.

that a maximum drain-source voltage will remain within the desired limits. Available GaN transistors have a maximum gate voltage of +6V. Situation is complicated by the fact that full enhancement of the GaN is achieved at gate voltage higher then +4V. So it is advisable to have voltage regulation in the gate drive circuitry.

III. Design and Analysis

The goal is to design the resonant reset forward converter using Gallium Nitride transistor and synchronous rectification. Achieving the efficiency as much as possible around 90% is the primary objective. We will choose the switching frequency to be around 320 kHz, which is a compromise between the efficiency and size. Knowing that, a good choice of a transformer and the inductor core is RM4, N49 material from TDK.

Design input parameters are given in Table I.

TABLE I
DESIGN INPUT PARAMETERS

		Min	Typ	Max	
Input voltage	V_{IN}	18	24	36	V
Output voltage	V_O		5		V
Output current	I_O	0.1	2		A
Output current limit	I_{OCL}		2.4		A
Full load efficiency	η		90		%
Switching frequency	f_{SW}		320		kHz

Starting from design input parameters we will now calculate basic parameters for the transformer and output inductor (Table II).

TABLE II
TRANSFORMER AND INDUCTOR INPUT PARAMETERS

		Max	Typ	Min	
Duty cycle	D	0.43	0.32	0.21	
Core cross sect. area			0.11		cm^2
Core effect. volume	V_E		0.29		cm^3
Prim. RMS current	I_{PRMS}	0.99	0.85	0.69	A
Sec. RMS current	I_{SRMS}	1.31	1.13	0.92	A
Flux density	B_{pp}		182		mT
Specific core losses	P_V		0.3		W/cm^3
Number of prim. turns	N_P		12		
Number of sec. turns	N_S		8		
Primary resistance	R_P		55		mΩ
Secondary resistance	R_S		29		mΩ
Output inductance	L		21		μH
Number of ind. turns	N		12		
Air gap required	g		0.1		mm
Winding resistance	R_L		27		mΩ

Now we can wind the transformer and output inductor prototype. We will use for the primary three parallel strands of 0.3mm enameled copper wire and for the secondary a bundle of seven 0.15mm wires twisted around each other, in order to keep the AC resistance low as much as possible. For the output inductor we will use 3 parallel strands of 0.3mm enamelled copper wire.

Knowing RMS currents and specific core losses we can now calculate the losses in both magnetic components (Table III). Total transformer power loss at 24V input voltage is 164mW. This results in approximately 20°C rise above ambient temperature. The temperature rise on the inductor is 13°C. Satisfied with the results, the optimization of a transformer and inductor is not necessary.

TABLE III
TRANSFORMER AND INDUCTOR OPERATING PARAMETERS

		Max	Typ	Min	
Thermal resistance	R_{TH}		120		K/W
Core loss	P_{CORE}		87		mW
Primary loss	P_{PRI}	54	40	26	mW
Secondary loss	P_{SEC}	50	37	25	mW
Total transformer loss	P_{TOT}	191	164	138	mW
Inductor RMS current	I_{LRMS}		2		A
Inductor loss	P_{IND}		108		mW

For higher efficiency, the current sense resistor is biased, reducing the current sense amplitude, so it can be three times smaller. As a result we have smaller power loss. Power dissipated in current sense resistor is given in Table IV.

TABLE IV
CURRENT SENSE RESISTOR POWER LOSSES

		Max	Typ	Min	
Current sense resistance	R_{CS}		165		mΩ
CS resistance loss	P_{CS}	162	119	79	mW

Power switch losses can be expressed by the equation

$$P_{FET} = P_{COND} + P_{ON} + P_{OFF} + P_{QOSS} \quad (3)$$

where

P_{COND} is the conduction loss given by

$$P_{COND} = I_{RMS}^2 R_{DS} \quad (4)$$

P_{ON} is the turn-on switching loss given by

$$P_{ON} = \frac{V_{DS} I_P (Q_{GS} + Q_{GD}) f_{SW}}{2 I_G} \quad (5)$$

P_{OFF} is the turn-off switching loss given by

$$P_{OFF} = \frac{V_{DS} I_P (Q_{GS} + Q_{GD}) f_{SW}}{2 I_G} \quad (6)$$

and

P_{QOSS} is the capacitance charge loss given by

$$P_{QOSS} = \frac{Q_{OSS} V_{DS} f_{SW}}{2} \quad (7)$$

For the primary switch Q we choose a Gallium Nitride transistor EPC2016. Using Eq. (3) to (7) we have calculate his operating parameters that are given in Table V.

TABLE V
PRIMARY GAN FET OPERATING PARAMETERS

EPC2016		Max	Typ	Min	
Drain-to source voltage	V_{DS}	100			V
ON resistance	R_{DS}	15			mΩ
Gate-to-drain charge	Q_{GD}	11			nC
Gate-to-source charge	Q_{GS}	5			nC
Output charge	Q_{OSS}	20			nC
Conduction loss	P_{COND}	23	17	11	mW
Switching loss	P_{SW}	67	90	134	mW
Total loss	P_{TOT}	85	103	143	mW

Peak stress on the forward and freewheel synchronous rectifier will be less than 30V, therefore we will use IRF7468 MOSFETS. Their operating parameters are given in Table VI.

TABLE VI
FORWARD AND FREEWHELL SYNCH MOSFET OPERATING PARAMETERS

IRF7468			Typ		
ON resistance	R_{DS}	12			mΩ
Q_1 RMS current	I_{Q1RMS}	1.31	1.13	0.92	A
Conduction loss	P_{CON}	31	23	15	mW
Q_2 RMS current	I_{Q2RMS}	1.39	1.39	1.39	A
Conduction loss	P_{CON}	35	35	35	mW

As a freewheel diode D we will use Schottky diode MBRS140 with operating parameters given in Table VII.

TABLE VII
FREEWHEEL DIODE OPERATING PARAMETERS

MBRS140			Typ		
Forward voltage drop	V_F	0.55			V
Dwell duty cycle	D_{DWELL}	0.05	0.16	0.27	
Peak current	I_{PEAK}	2	2	2	
Conduction loss	P_{CON}	55	176	297	mW

IV. REALIZATION

DC/DC converter was built on FR-4 substrate with 70μm copper. For optimal performance low side driver LM5114 is used with GaN FET. Also we have used simple gate drive circuit for synchronous rectifiers.

Using resistive load we have measured full load efficiency at various input voltages. The results are given in Table VIII.

TABLE VIII
EFFICIENCY

			Typ		
Input voltage	V_{IN}	18	24	36	V
Input current	I_{IN}	0.608	0.464	0.319	A
Input power	P_{IN}	10.944	11.136	11.484	W
Efficiency	η	91.37	89.8	87.08	%

The drain voltages of the primary power switch are recorded using Digital Phosphor Oscilloscope TDS5052, at full load and input voltages of 18, 24 and 36V are given in Figs. 3, 4 and 5 respectively.

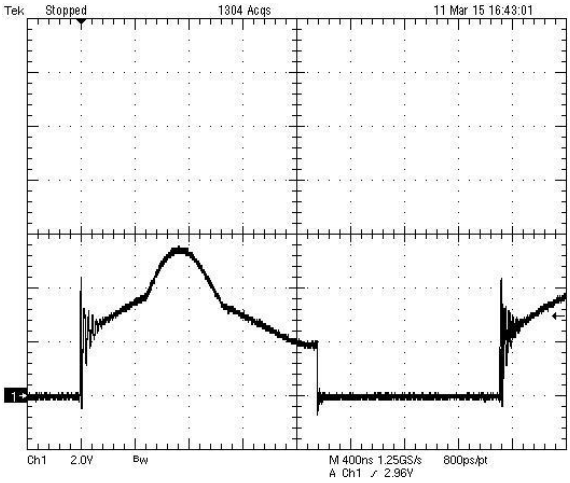

Fig. 3. Drain voltage waveform at 18V

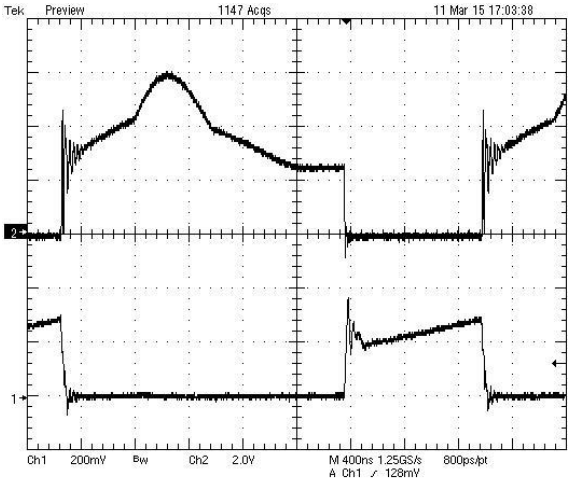

Fig. 4. Drain voltage waveform at 24V

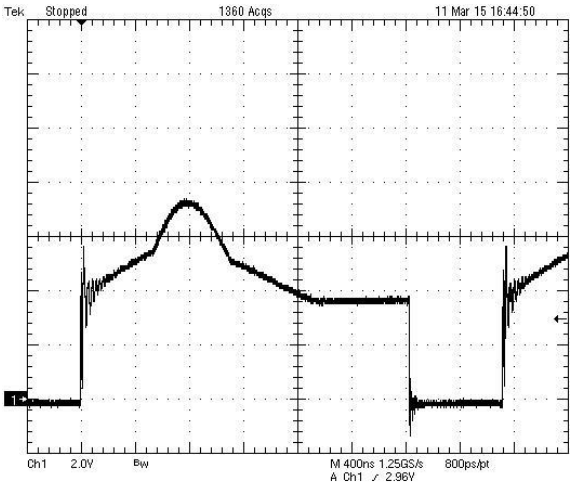

Fig. 5. Drain voltage waveform at 36V

The turn-on and turn-off waveforms for GaN FET are given in Figs. 6 and 7.

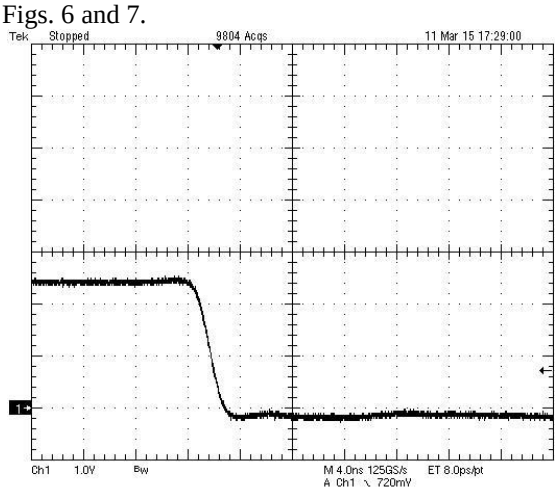

Fig. 6. GaN FET turn-on waveform at 24V

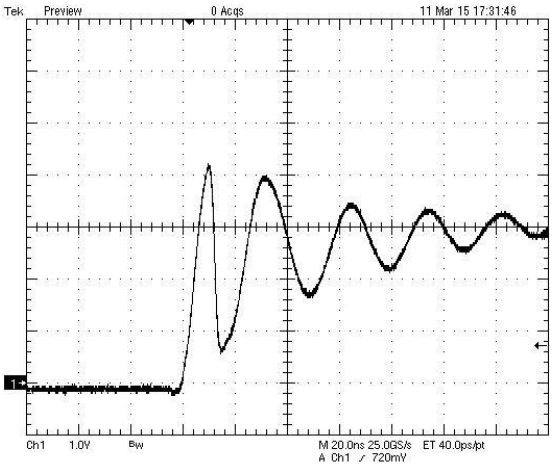

Fig. 7. GaN FET turn-off waveform at 24V

Gate and drain voltage waveforms of the forward and freewhelling rectifier are given in Figs. 8 and 9 respectively.

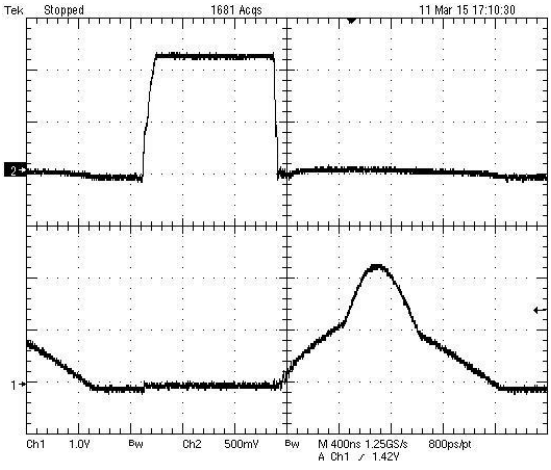

Fig. 8. Forward rectifier waveforms

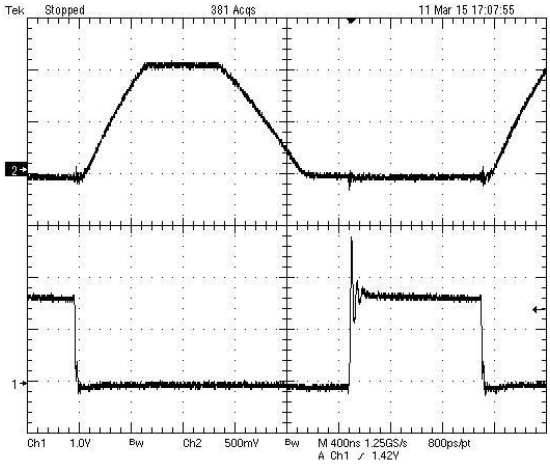

Fig. 9. Freewhelling rectifier waveforms

The picture of the converter prototype is given in Fig. 10 .

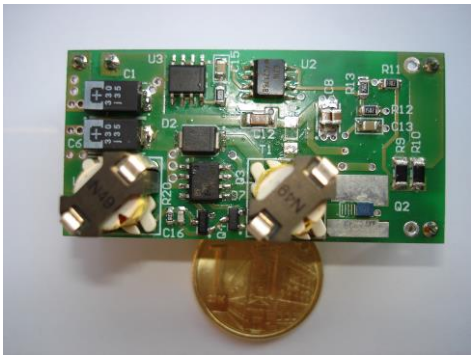

Fig. 10. Converter prototype

V. Conclusion

In this paper the design and analysis of resonant reset GaN forward converter with synchronous rectification is presented. The prototype was built and tested. The results verified that the full load efficiency is around 90%.

Acknowledgement

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