Mathematical model of control system based on programmable environment

Anatolii Aleksandrov [1], Goran Goranov [2], Pavel Hubenov [3]

Abstract – **The purpose of this article is to show consistency in implementation of the control system of a machine based on a programmable logic. It starts with a clarification of the requirements which determining its functionality and move on with calculation of a mathematical model of each block. The algorithm and the choice of the programmable environment for implementation are a topic of another article. Analysis of researched results.**

Keywords – **Logic gates, Control system, PWM, CPLD.**

I. INTRODUCTION

For reliable engineering sizing and implementation of a control system is extremely important to clarify the requirements which is based on. They are determined by industry, functionality, complexity, till the level of operators and lots of other factors but in conclusion – by the customer. In turn, requirements set the rules by which it will be designed and implemented - electric power modes, speed, management modes, to determine the nature and essence of each piece separately. The purpose of the designed machine is to drill holes and winding the thread in aluminum details.

Its principle of operation is as follows: the aluminum detail is placed in a magazine, loaded into the conveyor, transport towards a position, where the detail is preciously positioned, drilled by "Station1" for two holes, transported to the next position to the "Station2", wherein the cut thread, and exported by the conveyer. Then the cycle is repeated.

The operating accuracy of the machine depends on mostly of the accuracy of the angular displacements. There are few approaches for their realizations. The simplest block diagram is shown on Fig.1, a). An advantage of the method is easier to maintenance the system in time and at a lower cost. The disadvantage is the lack of feedback to control the speed by direct data delivery in case of faults situation. Tracking the speed of the shaft directly is impossible, and everything depends on the accuracy of microprocessor driver and the constant load. The only way to observe the statement of the motor is by consumed current. It is widely used in packaging machines with stretch film. [1, 2]

Second method includes feedback realized by three Hall sensors, installed at 120 °, which allows the monitoring of the speed and direction of the motor shaft. The advantage of this configuration is the timely reaction of the driver in the event of faults situation. Also, the motor speed can be controlled by managing more precise and reaction on time, even if the load is dynamic, Fig. 1, b). It is used in the management of conveyors or drives with frequent changes of direction or speed. [3, 4]

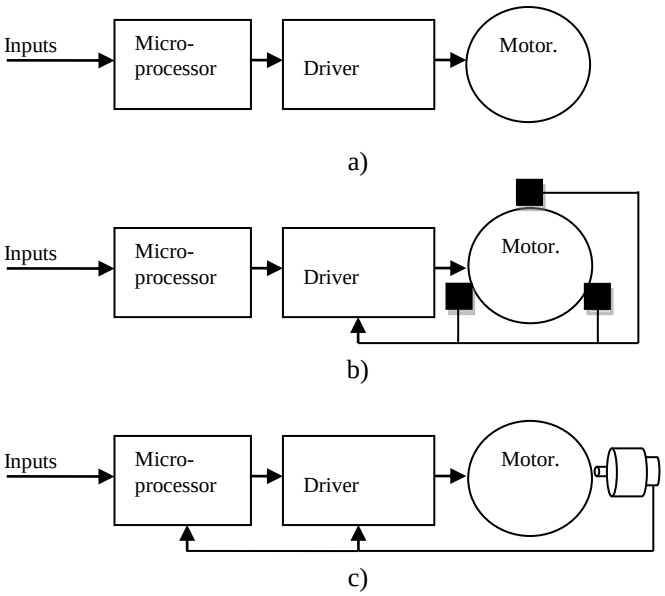

Fig. 1. Basic motion solutions

The most precise of the three configurations is shown in Fig. 1, c). The shaft is coupled with an encoder (photoelectric converter). Its function is to convert the angular displacement in a pulse sequence, i.e. pulses are corresponding to just one turn of 360 °. Basically pulses per round are multiple of 2^n. There are exceptions, such as those with resolution 200, 400 or more pulses per turnover. For precious tracking the location of the shaft is necessary installation of a sensor for a specific referent point. In this case, the microprocessor looks for this signal and launches counting pulses from the converter. For achieving this goal can be used the embedded in the encoder reset pulse, which is only one for a turnover. The disadvantage of the approaches with sensor or reset pulse, the error that occurs due to the timing of engine braking and the subsequent vibration. When positioning is critical, processor permanently monitor this pulse sequence, ready to stop the cycle of operation of the machine and put the alarm. It can be avoided by using a delay circuit ensuring a delay. The time delay method allows the signal of the sensor to be delayed within a few pulses or time respectively few microseconds. [5]

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Even better positioning is achieved using absolute encoder. Differentiations from the previous one is that each position corresponds to a set of *n*-bit digital code. In this way positioning is sufficiently precise because every single position defines data which is unique. Although power supply interruption could occur, the position will be remembered and the cycle resumes without failures.

The provided data is usually in binary code 8-4-2-1 but higher noise protection can be achieved easily when output data is in Gray code. This method of control allows the realization of dynamic brake at which the processor supports the entire drive unit in a stable stationary. These are so-called servo systems. Widely applicable at positioning of robots, CNC class machines, confection cutting machines and extruders in polyethylene industry, and more. [6]

To ensure correct positioning of components, set system requirements determine the type of approach used and the specific drivers and their associated control units.

II. MATHEMATICAL MODEL OF THE BASIC MODULES

When the requirements are completely fixed, has to design the plan for algorithm design. The more detailed it is, the more easily design of as small as possible modules regarding the functionality.

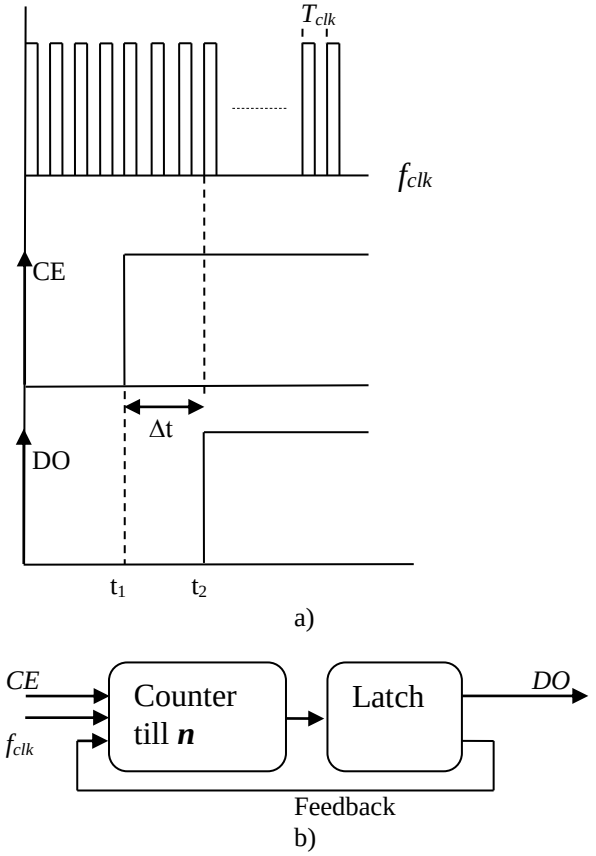


Fig. 2. Transition diagram and schematic of a delay line

Thus, by making easier for synthesis modules is achieved faster integration in a complex system, quick add or remove functionality and easier debugging. Using this approach, the main types of circuit solutions are simplified to next four modules - Time Delay Line, combinational scheme with X-input and Y-output (Code Converter), Digitally Controlled Frequency Generator, Pulse Width Modulation Generator.

1. Time Delay Line

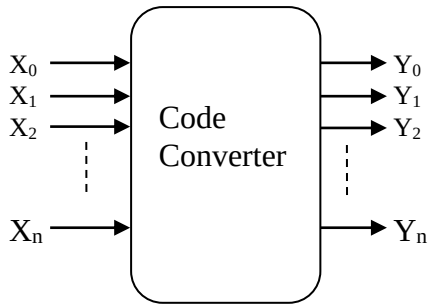
The block diagram of the delay line circuit is given in Fig.2, b). It provides accurate time delay. The difference between the received input signal and delayed output one is

$$\Delta t = t_2 - t_1 = n.T_{clk} \text{ [sec]}, \quad (1)$$

where n is the number of periods which the counter has to count and then triggers the latch, fig.2, a). The latch itself ensures a stable and resistant statement and as per the feedback blocks the clock frequency pulses.

2. Code Converter

The second module Code Converter is shown in Fig. 3. Basically it is a combinational circuit which provides output binary data according to the input binary data. Applicable when switching relays, e.g. controlling a pneumatic distributor, a pump, a fan, etc., based on the input performance of various conditions. They could be driven by signal of active sensor, limit switch, or signal for completed cycle of a previous module within the algorithm. This kind of block has from one to lots of number of outputs depending on its application - provide simultaneously enable or disable output signal towards other modules.



X_n	…	X_1	X_0	Y_n	…	Y_1	Y_0
$[CS_n]$		$[SS_1]$	$[CE]$	$[t+1]$	$[t+1]$	$[t+1]$	$[t+1]$
0		0	0	0		0	1
		⋮				⋮	
1	1	1	1				

b)

Fig. 3. Schematic and diagram of Code Converter

The state transition diagram is shown in Fig. 3, b) where in the left side are filled input magnitudes and in the right side are output ones corresponding to the adjacent input sets. The right side is the statement in the next moment $t + 1$. Left located sets could be different conditions (for example: CS_n – Control

Signal *n*, SS_1 – Signal Sensor 1, *CE* – Control Enable), which will provide signal for execution. Mostly converters owned a large number of input signals - 1 till 10 an above, but could be used only strongly defined sets. In this case, the synthesis must take into consideration that such a function is incomplete and should be threat using an extra approach to avoid unacceptable switching. They are in relationship to the statement so called "not defined" which has to be include in the synthesis. When the outputs are more than one, every single one has to be synthesized by minor members into separate own table using Karnaugh or Veitch mapping output equation, which is converted to the preferred type of basic logic units – AND-OR, NOR, or NAND. Finally, subsequently schemes for different outputs are combined into a common combinatorial scheme. [7]

3. Digitally Controlled Frequency Generator

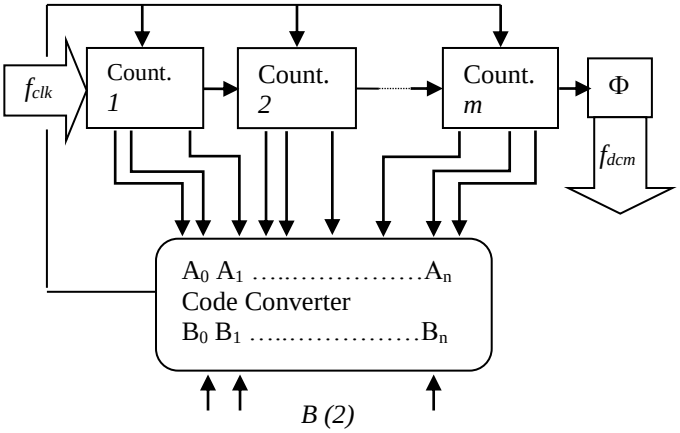


Fig.4. Block schematic of frequency generator

Block schematic of the generator is displayed in Fig.4. Generally, it is useful for frequency control of stepper motor's driver. The driver is allowed to control the motor by micro steps, i.e. a defined number of pulses is needed to be realized one complete revolution of the motor shaft. For example, the selected driver has a maximum number of 51200 steps per revolution, which means that a 360 degrees' rotation will be reproduced by 51,20kHz for just a second. Since this engine drives a conveyor and does not work in synchronization with another one, the requirements for it does not obligate the frequency to be exactly an integer than to be stable in time. This is the reason lead to the choice of this approach for implementing the control scheme. Otherwise could be use other method when a phase noise is observed, but the frequency is an integer and can be changed in small steps, for example 1.0 Hz.

The output frequency is determined by the formula:

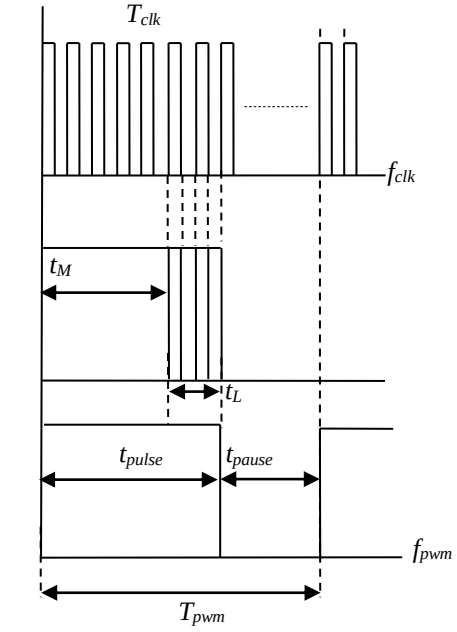
$$f_{dcm} = f_{clk} / B(10), \qquad (2)$$

where number *B* is in binary-decimal system, but is entered in binary code to the inputs of Code Converter. [8]

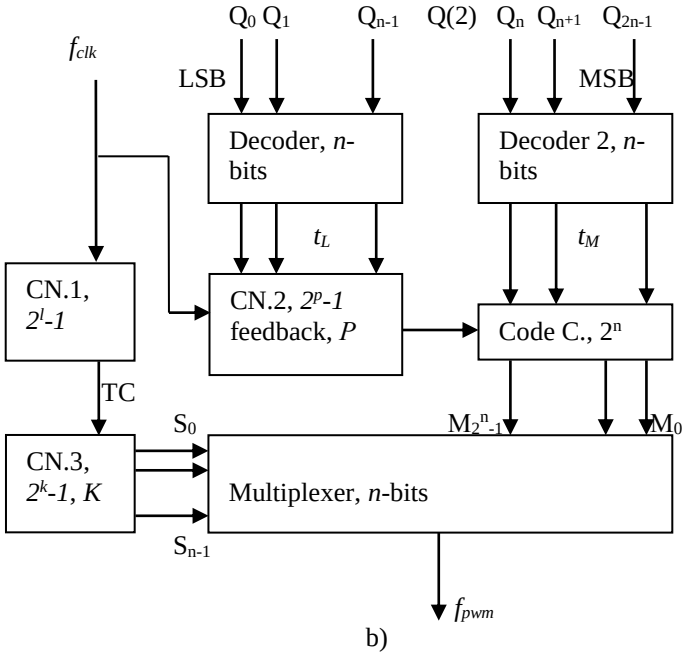
4. Pulse Width Modulation Generator

The approach for pulse-width modulation is given in Fig. 5, b). As per the block diagram of the generator, the more complexity the more precision of the duty cycle is achieved and the most capacity of programmable platform is available.

The principle of operation is as follows: multiplexer provides M_2^n number of channels, each of them is active for a defined time. It is determined by *l*-bit counter "CN.1", which counts the pulses of clock f_{clk}. This counter provides an output signal when overflow and switches counter "CN.3" which manages the address inputs of the multiplexer.



a)



b)

Fig.5. PWM generator

To realize the logical high level from the period T_{pwm}, Fig. 5. a) is used code converter "CC" which output code is code of

Johnson, providing a high level to the inputs of the multiplexer. It is managed by "Decoder 2" and "Code C" delivers to all junior multiplexer's channels, logical high level. For the current active channel of the decoder, "Code C" receives a signal from the other decoder. After counting the pulses from *p*-bit "CN.2" starts logical low level of the period T_{pwm}. That period of F_{pwm} is determined by the equation:

$$T_{pwm} = t_{pulse} + t_{pause} \text{ [sec]}, \quad (3)$$

where t_{pulse} is the time of the logical high level Fig. 5, a). This time is the sum of the other two:

$$t_{pulse} = t_M + t_L \text{ [sec]}, \quad (4)$$

as they are received from "Decoder 2" and "Decoder 1". Both decoders are managed separately by *n*-bit code, but connected as per their ranking by importance – starts with the most insignificant, LSB (*Low Significant Bit*) towards the most important, MSB (*Most Significant Bit*). The time specified by the decoder for the most significant bit (MSB) is:

$$t_M = (K\text{-}1).t(K) \text{ [sec]}, \quad (5)$$

where *K* is the number of the active channel of the multiplexer. Active time for each single channel is:

$$t(K) = 2^l . T_{clk} \text{ [sec]}. \quad (6)$$

The time specified by the decoder for the least significant bit (LSB) is:

$$t_L = P. T_{clk} \text{ [sec]}. \quad (7)$$

Here *P* is the number to which the external feedback of the counter "CN.2" is adjusted and then resets.

The step, or the quantum, by which the duty cycle of the pulse width modulated signal is determined is by the coefficients *k* and *l*:

$$Qu = 100 / (2^k . 2^l) \text{ [\%]}. \quad (8)$$

Duty cycle λ is determined by:

$$\lambda = (t_{pulse} / T_{pwm}).100 \text{ [\%]}. \quad (9)$$

The number Q, managing decoders and sets duty cycle, is the described as:

$$Q\ (10) = \lambda / Qu \text{ [\%]}, \quad (10)$$

then converted into binary and is provided to inputs Q_0 - Q_{2n-1}. The condition, which must be strongly obligated to be kept in the method of realization of the PWM signal is:

$$p \leq l. \quad (11)$$

Both mentioned generators in the above are designed so as to be controlled by binary parallel code. This approach allows changing the speed of the controlled motor to be performed from minimum to maximum within a single period of the clock frequency. It is useful whether the engine has a number of different speeds.

III. CONCLUSION

The approach of the control system implemented in the drilling machine is recognized by using easy synthesis of all types of modules. It allows the system to be designed and implemented sufficiently simply, efficiently and reliably. The platform successfully responses to the requirements is CoolRunner-II, with mounted programmable logic matrix XC2C256-7TQG144C. Used matrix delivers flexible enough base for fine adjustments during the revival of the system and subsequently in its implementation as control unit in real facility.

Differenced from other types of architectures of programmable devices, where the number and functionality of the various blocks are factory pre-determined, everything here depends entirely on the designer and made synthesis. The methodology combines mathematical model and synthesis through minimization of logic functions, allows the expansion of the control system with more than one programmable matrix to remain just as easily and reliably. The implementation of functional logic elements makes this approach applicable in almost all the developments of programmable logic controllers series of leading manufacturers. The advantage is much wider audience, unlike using any other language for programming. To be continued with second article which describes algorithm and realizations of logic gates schematics.

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