Problems and Properties of a Current Amplifier When Realized in Ultra Deep Sub-micron Technology

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Abstract – **In this paper are described three versions of a current amplifier and each of them is realized with FETs having different channel length: 90nm, 45nm and 30 nm. Their basic properties are simulated and discussed, demonstrating the major benefit of the shortening of the channel length – extension of the frequency bandwidth. The problems arising with the shorter channels length are also considered briefly.**

Keywords – **amplifiers, current mode operation, short-channel effects, MOSFET.**

I. Introduction

The scaling of the semiconductor devices in modern CMOS technology improves the performance, lowers the price and reduces the power supply of the fabricated circuits [1,2]. While device downscaling is driven primarily by the benefits it has in digital design, it introduces new effects in transistor behavior, which makes analog design challenging. As channel lengths decrease below 1μm, second order effects, which were not taken into account for long channel FETs must be accounted for. When short channel effects become significant the traditional analytic approach in analog design is not feasible [3]. This necessitates a modification of the existing analytic design methodologies and employment of new techniques.

Shrinking the gate length is accompanied by decrease in power supply voltage, which is a major issue in analog design. However threshold voltage does not scale as much as the supply voltage, and transistors are biased at lower voltages, which results in worse transistor properties [1,4].

Current mode operation overcomes some of the problems with downscaling because it requires lower supply voltage compared to its voltage mode counterparts [4,5]. It also has some other advantages – at low power supply voltage they allow wider signal dynamic range, wider frequency bandwidth, better linearity. For these reasons, current mode designs become very popular in many high performance analog and mixed signal applications – RF front ends, data converters, oscilatiors, etc.

The legacy design methodology applicable for long channel devices uses theoretical circuit analysis based on expressions taking into account only first order effects. In contrast, designing an amplifier in sub-micron technology must include the higher order effects, rendering a purely analytical approach no longer viable, since it leads to significant inaccuracies mainly related to the specific short channel effects – drain induced barrier lowering, channel length modulation, velocity saturation [1,3,4]. Even some technology specific parameters, e.g. μC_{ox}, are not constant anymore and depend on transistor geometry.

A method for design of a basic current amplifier, when short channel effects are significant is proposed in [6]. For the cases when short channel effects are moderate the design procedure gives very good matching between specification and simulation results. Further reduction of device sizes causes more and more deviation from the basic theory. The goal of this paper is investigation of these effects when the sizes approach the technology defined limits. A basic current amplifier is designed with different FET devices with different channel lengths: 90nm, 45nm, 30nm.

II. Brief Review of the Design Method

The circuit of a basic current amplifier is shown in Fig.1. The major problem in its design is the requirement of identical transconductances of M_1 and M_3 at the same drain currents. This is necessary in order to keep the symmetry in upper and lower halves of the circuit. The formulas for long channel device transconductance and drain current are [2,5]:

$$g_m = \mu C_{ox} \frac{W}{L} V_{ov};\ I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS}), \qquad (1)$$

where μ is the carrier mobility, C_{ox} is gate capacitance per unit area, W and L are channel width and length, V_{ov} is overdrive voltage and V_{DS} is drain-source voltage of the transistor. The widths of M_1 and M_3 should be connected with the *n*- and *p*-carriers mobilities by the relationship $W_1/W_3 = \mu_p/\mu_n$ in order to have equal g_m's of these transistors [6]. It follows from (1) and is valid for long-channel transistors only.

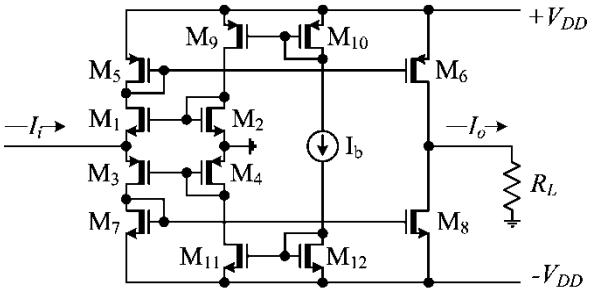

Fig.1. The circuit of the current amplifier

The above mentioned reasons do not allow to implement this relationship for short channel transistors. The design

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procedure proposed in [6] uses a graphical and analytical approach for initial design centering and then refining the device dimensions by parametric simulation. Firstly the dependences of g_m/W and I_D/W from gate-source voltage for PFET and NFET are plotted [2]. Short channel effects make these normalized curves slightly different. However the differences are small and will be compensated in the following optimization. The next steps are:

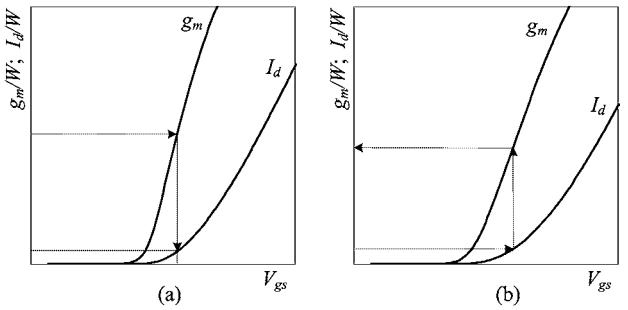

Fig.2. Plots of normalized g_m and I_D vs. V_{GS}: (a) NMOS; (b) PMOS.

1) The transconductance of the input transistors are defined by the input impedance:

$$g_m = g_{m1} = g_{m3} = \frac{1}{2.2R_i} \quad (2)$$

A normalized value of g_m for NMOS is chosen in the linear region of the curve (Fig. 2(a)). The width of the transistor can be determined by dividing the desired transconductance by the chosen value.

2) The normalized g_{m1} defines V_{GS} and the corresponding normalized value of I_{D1} of M_1. Since the width of M_1 is already known the required drain current of M_1 can be calculated.

3) The drain currents for M_1 and M_3 must be the same and equal to the total input branch current – $I_{D1} = I_{D3} = I_D$. Looking at Fig. 2(b) we pick a value I_{D3}/W in the region where drain current is a quadratic function of V_{GS}. This value also defines the V_{GS} and the width of M_3.

4) For the selected value of I_{D3}/W it should be verified that the corresponding g_m/W is in the linear region in Fig. 2(b). If it is not, another value of I_D/W should be chosen.

5) These steps do not guarantee the exact matching of g_{m1} and g_{m3} since the transistors are of different types. The received values will be used as initial for the following optimization based on parametric analysis, in which the values of g_{m1} and g_{m3} are equalized at the same drain current.

III. Problems Arising with Device Downscaling

To study the changes in the amplifier parameters and behavior, it is designed in 32nm bulk CMOS technology, developed for SRAM, logic and mixed-signal applications. Three versions of the amplifier are considered: 1) realized with hpar FETs with gate length of 90nm; 2) realized with slvt FETs with gate length of 45nm; and 3) realized with slvt FETs with gate length of 30nm (the minimum allowed drawn gate length for thin oxide in the used 32nm technology). The abbreviations hpar and slvt are for different types of MOS transistors in the Process Design Kit [7]. All three version are supposed to meet the following specifications:

- input impedance R_i<500Ω;
- power supply V_{DD}=±1V;
- current gain A_i equal to 1, i.e. current buffer.

The design is based on the procedure outlined in the previous section. All transistors are working in strong inversion in saturation and the corresponding DC branch currents are listed in Table 1.

TABLE I
DC CURRENTS IN THE AMPLIFIER BRANCHES

Current in μA through	I_b	M_5, M_1, M_3, M_7	M_9, M_2, M_4, M_{11}	M_6, M_8
Version 1	74	72.6	73.2	98.4
Version 2	93	79.3	85.7	121.5
Version 3	115	97.6	105.4	186

Several problems were faced during the design:

1) Due to channel length modulation the current mirrors ratios depend strongly on the drain-source voltage. Then the current gain deviates from the ratio of the areas M_5/M_6 and M_7/M_8 (the theoretical value of the gain). For example, if these transistors have equal areas, the gain for Version 1 is 1.18, for Version 2 it is 1.25, and for Version 3 it is 1.3. An accurate value of current gain can be achieved by varying the channel widths with parametric analysis.

2) Decreasing the channel length relatively reduces the back-gate transconductance g_{mb} concerning the main transconductance g_m. In [6] g_{mb} is estimated as more than 10% of g_m and its contribution is reflected in formula (2) by the factor 2.2. For shorter channels g_{mb}/g_m is less than 5% and this factor should be reduced to 2.1 or even 2.

3) The threshold voltage V_{th}, which is usually considered to be constant, in fact depends on the drain-source voltage V_{ds} due to drain induced barrier lowering (DIBL effect). This is a common short channel effect in FETs. The variation of the threshold voltage is investigated by simulation for the used transistors and the corresponding plots are shown in Fig.3.

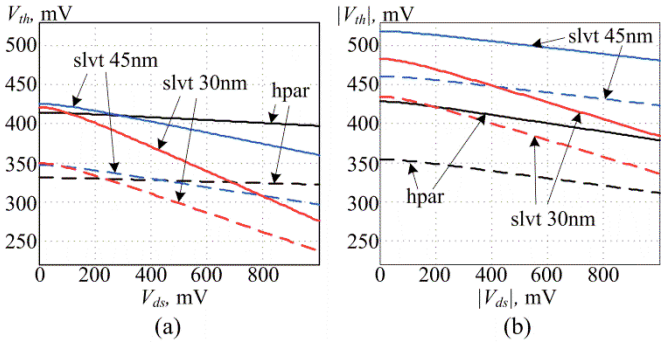

Fig. 3. Dependence of the threshold voltage from the drain-source voltage for the transistors of interest. Solid lines - with bulk effect, dashed lines - without bulk effects: (a) NMOS; (b) PMOS.

Several effects are observed in Fig.3. As expected, shorter channels have greater dependence of V_{th} on V_{ds}. Transistor type hpar is optimized for analog applications, which results in negligible difference of threshold voltages for PFET and

NFET and their deviation with V_{ds}. This is not the case for slvt FETs, which are basically intended for use in digital circuits – V_{th} has stronger dependence on V_{ds} and the difference between V_{th} of PFET and NFET is more than 20%. However overcoming the challenges in amplifier design based on slvt FETs proposes some significant benefits – small die area and operation at higher frequencies.

4) The breakdown voltages for the used transistors are low (1V) for all three types. On the other hand, threshold voltages are relatively high – up to 0.5V, while the circuit has four transistors in series in most of the branches. Both circumstances require operating at a total supply voltage, which is more than the limits of the transistors and here ±1V is used. To guarantee the safe operation it is necessary to check the voltages over transistors at different input current. The limits for the magnitude of the input currents are defined with the following procedure: a DC current source is applied at the input and its current is varied from -3mA to 3mA with DC sweep analysis. The plots of the voltages, which exceed the limits, are given on Fig. 4 for amplifiers with hpar and slvt 45nm. The corresponding plots for slvt 30nm are very similar to slvt 45nm and they are not shown. The maximum input current I_{imax} determined from the figure are: 1.2mA for Version 1 (hpar), and 1mA for Versions 2 and 3 (slvt).

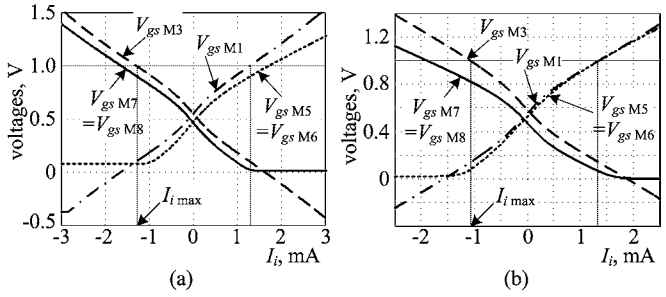

Fig. 4 Gate-source voltages, which exceed the safe operation range: (a) amplifier with hpar FETs, (b) amplifier with slvt 45nm FETs.

IV. Simulations of the Basic Amplifier Parameters

The three versions of the amplifier are compared by several basic parameters: small and large signal current gain, input impedance, and transfer characteristic (I_o vs. I_i) and THD. The small signal parameters are shown in Fig. 5. The current gain is different for the three versions for reasons commented above. More interesting are the frequency bandwidths. The corners frequencies are: 12.03 GHz for Version 1, 25.6 GHz for Version 2 and 45.9 GHz for Version 3. For comparison, the same amplifier designed with another type of MOSFETs from the same technology – zgfets with 270nm minimum gate length [6] has corner frequency of 2.3GHz. The benefit of using short channel transistors is obvious. The input impedance is close to the designed and it keeps its value up to few GHz.

The large signal behavior is illustrated in Fig. 6. They are obtained by parametric time domain analyses using sinusoidal input current source with parameterized amplitude. Its frequency is fixed at 10 KHz - low enough to avoid slew rate effects and suppression of the harmonics, generated in the amplifier, from its frequency response.

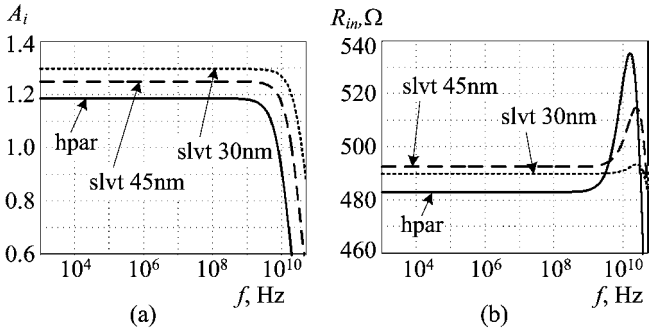

Fig. 5 Small signal characteristics of the designed amplifiers: (a) current gain; (b) input impedance.

The dependence of the amplitude of the output current from the amplitude of the input current is shown in Fig. 6(a). The curves are very close to each other due to the approximately equal current gains of all three versions and it is difficult to distinguish them. For this reason two other characteristics are added: large signal current gain $A_i=I_o/I_i$ and the THD, both as functions of the input amplitude. These characteristics show that the decreasing of the channel length increases the nonlinearity. Evidently this is the price for the extended frequency bandwidth. However, the amplifier with hpar transistors has similar THD as the amplifier with three times longer (270nm) zgfet transistors, which has 1.7% THD at I_i=1mA [6].

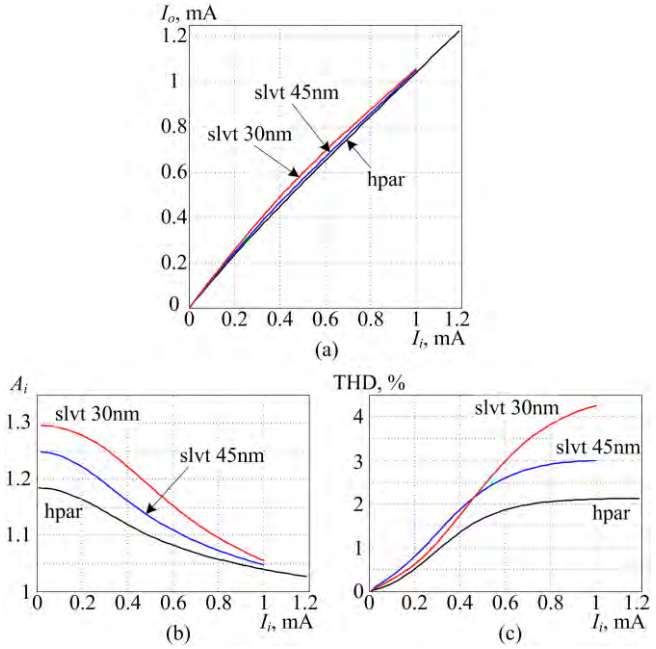

Fig. 6 Dependences of large signal parameters of the designed amplifiers from the input current: (a) output current; (b) large signal current gain; (c) THD.

V. CONCLUSION

One of the most common current amplifiers is designed with three different types of deep submicron MOSFETs from a 32nm CMOS technology: 90nm hparfet, 45nm and 30nm slvtfet. The major benefit of short channel transistors is significant extension of the frequency bandwidth – up to 45 GHz for the circuit with shortest channel transistors. The large signal behavior is also investigated and the hpar version of the circuit shows similar non-linearity compared to the same circuit with much longer transistors. Certain increase of the non-linearity is observed for the versions with shorter channel transistors (slvtfets). The maximum amplitude of the input current is lower due to the reduced operating voltages of the used transistors, but this limitation can be relaxed by using wider FETs and higher biasing current.

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