Power consumption evaluation of FPGA devices based on I/O and clock frequency

Marsida Ibro[1] and Luan Karçanaj[2]

Abstract – **In this paper, models to estimate and evaluate power consumption on FPGA devices will be introduced. FPGA-based electronic systems are becoming more attractive due to reconfigurability and high performance. Due to better fabrication techniques, nowadays FPGA elements contain many programmable blocks CLB (Configurable Logic Blocks) and other functionalities such as memory chip (on-chip memory), DSP blocks, clock synthesizer etc. But before the design of complex electronic systems is more valuable to make evaluations and estimations on power consumption. In order to make the right evaluation we have taken into consideration the internal resources like I/O and clock frequency, due to the complexity and design of such architectures. To achieve these goals, we will take into account other factors and results will show that the power consumption is reduced.**

Keywords – ***FPGA, Power consumption, Power consumption estimation, Power consumption models, I/O and Operation frequency***

I. Introduction

Field programmable gate arrays (FPGAs) provide an alternative solution for intensive calculations in digital signal processing applications (DSPs). The FPGA structure consists of two main components: logic blocks that implement the combinatorial part of on-chip memory design and memories. Logic blocks include Look-Up Tables (LUT) and information storage elements. These two elements found in configurable logic blocks (CLBs) make the FPGA architecture ineffective.

FPGA devices can be used to implement many applications with high throughput, but high performance and power consumption remain today's challenge for electronic systems, mainly on mobile devices. In this paper, methods that help estimate power consumption based on I/O (input/output) and operation frequency will be presented. In FPGA elements we need to take in consideration dynamic power which is the power consumed only when the transistors are working or not working (idle). Dynamic power loss is proportional to the number of transistors.

Due to the requirements for designing DSP systems, programmable logic devices are becoming very necessary. Programmable logic devices, such as FPGAs, offer high performance and therefore are faster than the traditional microprocessors. The reconfigurability of FPGA devices requires the usage of many internal hardware components.

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To implement a logic circuit on FPGA devices we need to use more transistors compared to ASICs (Integrated Application Specific Specifications). This leads to higher power consumption in FPGA and this is one of the areas where ASIC are superior to FPGA. As FPGA devices have higher power consumption, today is one of the main areas of scientific research.

In order to optimize power consumption of FPGA devices we can use CAD (Computer-Aided Design) architectures and circuits. The main focus for manufacturers and scientific researches related to FPGA and CAD, is to improve efficiency and performance [1, 2, 3].

Dynamic power is consumed as a result of the toggle rate in logic circuit signals during operation. These transitions increase not only in proportion to logic transitions activity of the signals in the circuit but also the charging / discharging of capacitors. Power leakage occurs even when circuits are in the idle state. Power consumption optimization and reduction of FPGAs offers many advantages because most of the today's applications are portable or battery-powered and mobile applications have limited standby power in some μA.

II. FPGA Architecture

FPGAs are built-in configurable circuits that can be used to design digital circuits. FPGAs configuration is done with VHDL (VHSIC Hardware Description Language) or Verilog programming languages. FPGAs contain configurable logic blocks that provide reconfigurability and programmable interconnects hierarchy is shown in Fig.1.

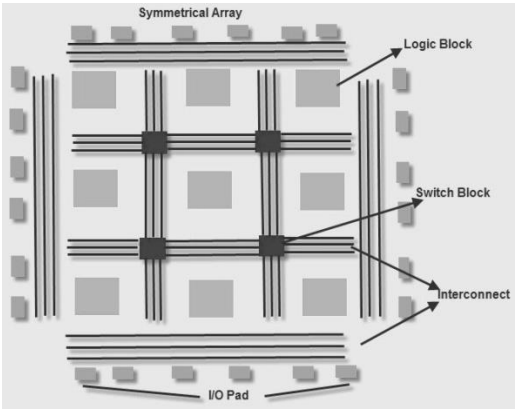

Fig. 1. FPGA architecture

The trends in terms of FPGA architectures technology comprise components such as DSP blocks, processors, and high-speed transceivers to realize the System On a Programmable Chip (SoPC).

In FPGA, connections between elements are realized by elements such as SRAM (Static Random Access Memory), flash cells or EEPROMs (Electrically Erasable Programmable Read-Only Memory) that directly connect components via interconnections.

III. Related Works

Nowadays, reducing power consumption and dynamic power leakage is a challenge on FPGA-based circuit design. One of the most effective techniques is to use partial reconfigurability. FPGA power consumption can be optimized even at the architectural level. The pipeline stages can reduce power consumption by about 25% to 40% [4, 12].

Reducing power consumption due to reconfigurability in FPGA-based DSPs is done by reducing unnecessary calculations from internal resources [5, 6]. Since FPGA architecture uses CMOS (Complementary Metal-Oxide-Semiconductor), a three level architecture is proposed for transistors. Also, different logic blocks structure using 4-LUTs with 3-inputs with multiplexers and DFFs (D flip-flop) can be used [7, 8, 9, 10].

IV. Methodology

To achieve accurate predictions, probability techniques are used, which are based on the conditions of transitions activity estimation for logic circuits. To reduce power consumption, following internal components have been taken into consideration like logic cells (LUT, flip-flops, and registers), interconnections, I/O cells, clock frequency and memory. The method used to measure the power consumed by any internal component in FPGA is:

1. Initially, we take the simplest case with the minimum number of elements, fixed toggle rate (12.5%) and constant room temperature.
2. While considered internal elements are variable, other components are constant to view the direct impact of each FPGA internal component. This procedure is accomplished using simulators software`s of each manufacturer.
3. The first element to be measured is interconnection because is used to make logic or I/O connections.
4. Finally, the procedure is repeated for each element. The measurement results from the proposed models are compared with the models of the manufacturers and will help to understand which components should be considered for reducing power consumption.

After using our methods, we will compare the results with those of the manufacturer's models as shown in Fig.2. To make the measurements we have used Spartan 6 kit board and Xilinx ISE Design tool. Xilinx Spartan-6 FPGA (XC6SLX9-TQG144) has 9152 logic elements, Onboard I2C serial EEPROM 24C04, MAX232 serial communication transceiver and 50 MHz Oscillator.

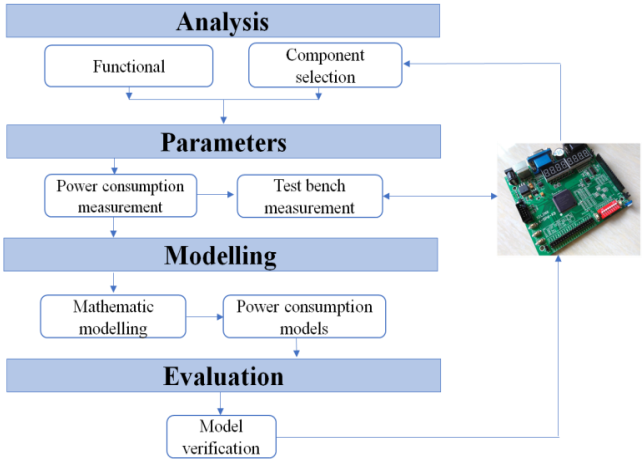

Fig. 2. Evaluation and measurement methods

V. Proposed Models for Power Consumption

Now, we will introduce commonly used methods to calculate, and estimate power consumption. These methods usually use probability estimates for glitch detection and then apply the glitch reduction method using flip-flop with negative triggering impulses. Before we define the models for power consumption will use the vendor measurements shown in Fig. 3.

As mentioned before, delays caused by logic gates can be risky when this function is used to control clock impulses. Most of the models used to explain power consumption for integrated IC circuits are based on equations derived from the CMOS inverter analysis [11].

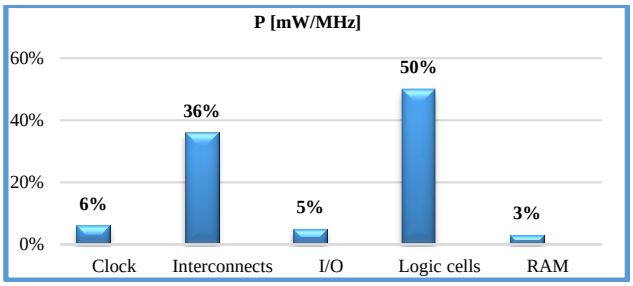

Fig. 3. FPGA components power consumption measured by vendors

In Eq. 1 is calculated the saturation current in PMOS (p-channel MOSFET) and NMOS (n-channel MOSFET) transistors:

$$I_{DSp} = -\beta_p \left[(V_{IN} - V_{DD} - V_{Tn})(V_o - V_{DD}) - \frac{1}{2}(V_o - V_{DD})^2 \right]$$
$$I_{DSn} = \beta_n \frac{(V_{IN} - V_{Tn})^2}{2} \quad (1)$$
$$\beta_p = k_p \frac{W_{eff}}{L_{eff}},\ V_{GS} = V_{IN} - V_{DD},\ V_{DSp} = V_o - V_{DD}$$

where W_{eff} is channel effective width, L_{eff} is channel effective length, k_p is a parameter that depends on process. This factor is calculated $k_p = \mu C_{ox}$, where C_{ox} is oxide capacitance for unit length and $C_{ox} = \varepsilon_0 / l_{ox}$, where l_{ox} is oxide width of CMOS gate. V_{Tn} is threshold voltage for MOSFET transistor, V_{GS} is gate-source voltage, V_{DD} is supply voltage in

drain terminal and V_{IN} is input voltage. In Eq. 2 is calculated the static power:

$$P_{static} = P_{leak} + P_{dp} \quad (2)$$

Dynamic power is calculated by the equation Eq. 3:

$$P_d = \frac{C_L \cdot V_{DD}^2}{T} = C_L \cdot V_{DD}^2 \cdot f \quad (3)$$

where f is clock frequency.

Dynamic power consumption and I/O power dominates overall total power consumption on FPGA. Often FPGAs designs require usage of higher clock frequency f. I/O commutation for high speed data and logic switching for larger frequencies became the dominant factors in power consumption for FPGA elements [12]. To effectively reduce total FPGA power, both static and dynamic power must be addressed while ensuring the FPGA's performance still meets design requirements. Xilinx mathematical model for power consumption is:

$$P = (M \cdot C \cdot tog_{LC} \cdot f_{max} \cdot P_{CLB}) + (G \cdot f_{max} \cdot P_{CLK}) + (L \cdot tog_{LC} \cdot f_{max} \cdot P_{LL} \quad (4)$$

where M is the number of flip-flops per CLB, C is the number of CLBs, tog_{LC} is toggle rate, f_{max} is maximum clock frequency, P_{CLB} is power to frequency ratio of the CLB, G is the number of global clock, P_{CLK} is power to frequency ratio of the global clocks, L is the number of long lines and P_{LL} is the power to frequency ratio of the long lines.

Dynamic power consumption source is the current needed for load capacity LC charging/discharging. The average dynamic power P_d required to load capacitance charging /discharging LC during clock period T is given in Eq.5:

$$P_d = \frac{1}{T}\int_0^T i_o(t) \cdot v_o(t)\, dt \quad (5)$$

An extra power loss is caused due to the short circuit current. This current depends on the rising edge and input voltage drop. If we assume that the rising and falling edge are equal, the power consumed by the short-circuit current is given in the Eq.6:

$$P_{SC} = I_{mes} V_{DD} \quad (6)$$

Another equation relates short circuit power for short circuit is also proportional to the frequency of operation. Short-circuit power consumption is reduced by about 20% of the total power consumption and will be given in Eq.7:

$$P_{sc} = \frac{\beta}{2}(V_{DD} - 2V_T)^3 \tau f \quad (7)$$

Input/output (I/O) elements allow logic circuits in FPGA devices, to communicate with external devices. I/O circuits are important because can limit the speed of the circuit and power consumed. There are several types of I/O circuits, such as input and output buffers, clock distribution, a clock buffer, and low-swing I/O [13, 14]. For circuits that contain several I/O, dynamic power consumption is calculated in Eq.8:

$$P_{input} = \alpha \cdot N_i \cdot E_{ii} \cdot f \quad (8)$$

where α is transition states, N_i the input numbers, E_{ii} is internal energy in W/Hz and f is operation frequency. Dynamic power consumption by the output circuit is expressed in Eq.9:

$$P_{dinamike} = \alpha\left(N_o E_{io} + N_o C_o \cdot {V_{DD}}^2\right) \cdot f \quad (9)$$

VI. Results and Discussions

A critical element in electronic circuits reliability is that a part of power is transformed in heating during the operation. Thermal characteristics of a circuit depend on equipment and used packaging, operating temperature, and operating current. Although these two factors, the power and time of the delay, are related to each other, differ in function of the power supply voltage. It is therefore very important to predict the performance with the increase of the delay time when the food source is reduced. This is important since the use of food resources at the level. low impact on the reduction of power consumption. Using the ring oscillators, we measure the current, voltage over frequency to obtain the maximum delay when using the lowest possible supply voltage.

Fig. 4 shows the block diagram of the ring oschillator which will be used for Spartan-6 device.

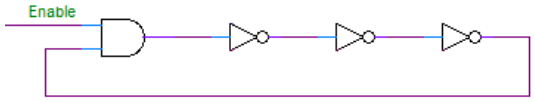

Fig. 4. Block diagram of ring oscillator

To measure the power consumed we follow the steps below: 1) we estimated power consumption of the designed circuit, 2) we calculated the maximum power for the device and 3) packaging and compare it with the estimated power values and with power measured by manufacture simulator. Based on the mathematical models we have used Xilinx ISE Design to make a comparison between our models and the manufacture tools to evaluate power consumption.

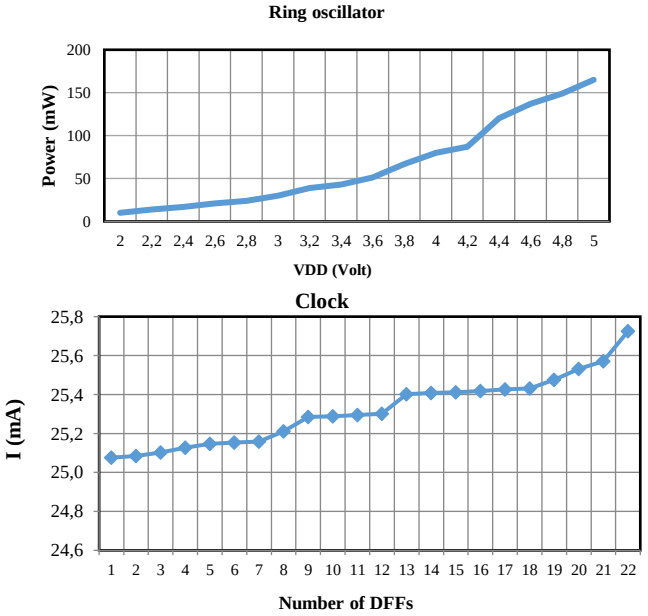

Fig. 5. Power measurements for different supply voltages and Current measurements of the clock signal for different used number of DFFs

After the measurement on the FPGA board, we have compared the result between the two methods. In Fig. 6., we can see the results taken from the methodology used to analyze and measure the power consumption of the main components in the architecture of the FPGA devices.

Fig. 7. shows power consumption of I/O components over the supply voltage. These measurements are done to get a whole picture about the effects of the inputs/outputs and to understand potential consideration in using models for estimation of power consumption.

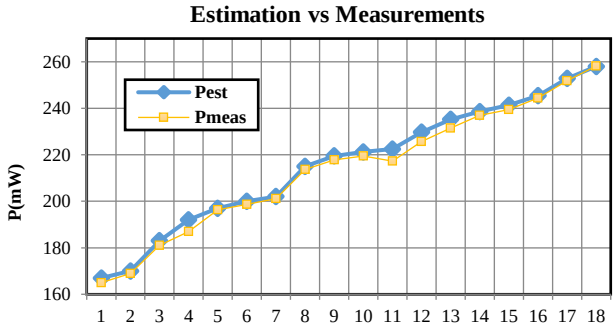

Fig. 6. Comparison of estimated and measured power consumption

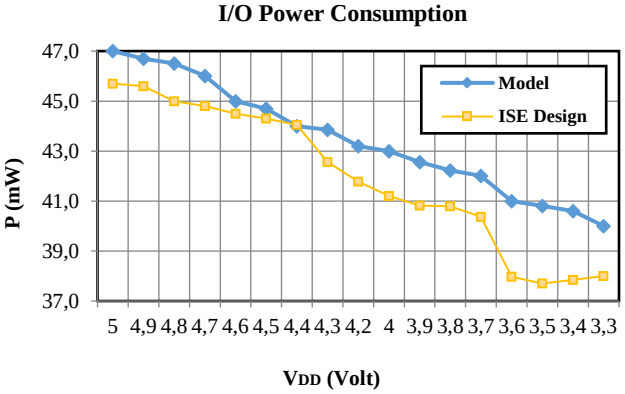

Fig. 7. I/O Power consumption

VII. Conclusion

FPGA architectures are composed of different electronic structures, such as CMOS, Pass-Transistor and SRAM. The power consumption behavior of such devices is much more complex than the power behavior of only CMOS circuits. In this paper, we have take in account, static power, dynamic power and short-circuit currents can be negligible. In FPGAs, power behavior should have a non-negligible DC component due to direct path currents that increase because of the pass-transistor structure, and due to leakage currents, that become important when increasing the number of equivalent ASIC gates. Results show that our measurements on power consumption models are good because they estimate power dissipation and show that power consumption depends on clock frequency and the number of logic cells used to design applications.

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