Teaching Methods for Digital Phase Locked Loop

Dimiter Badarov[1] and Georgy Mihov[2]

Abstract –**This article discusses the methodology, the tasks, the material base and the problems in the teaching process of all digital phase locked loop. Different types of phase and phase-frequency detectors are examined. Their parameters are compared and the advantages and drawbacks for different applications are discussed. Different types of digital integrators and digital filters are developed and tested along with the different phase-frequency detectors. Different circuits for Digitally Controlled Oscillator are developed and tested. Several different phase locked loops are built and tested. Their parameters are compared and discussed.**

Keywords –**All Digital Phase Locked Loop, Teaching methodology, Phase-frequency detector, Digitally Controlled Oscillator, FPGA.**

I. Introduction

The application of Phase Locked Loop (PLL) in the modern electronics is very wide. Along with the Direct Digital Synthesis (DDS) it is one of the main methods for generating clock frequencies. One of the advantages of the PLL is that it uses one reference clock frequency. The stability of the generated frequencies is equal to that of the reference frequency. The wide application of the phase locked loops requires more detailed examination. While the standard analog PLL are well examined and their development is almost finished, their digital equivalent can offer some advantages which require more attention. All structural blocks of the analog PLL are replaced with their digital functional equivalents. The transition to the digital electronics gives the advantages of easy testing using programmable logic devices and lowers the cost of the system. Although the development of the digital equivalents of the analog blocks offers some freedom for different solutions with better properties. Due to that a different solution for every block is developed, and a series of tasks are proposed for the education:

- The dependence of the digital code at the output of the digital integrator from the phase difference between the two input signals is examined for the different phase detectors.
- Different types of digital integrators and filters are proposed and the PLL stability is examined with them. The advantages of the different solutions are discussed.
- The different methods for Digitally Controlled Oscillators (DCO) construction are examined. The advantages for the different applications are discussed.

All of the proposed schematics are implemented and tested on Field Programmable Gate Array(FPGA)device Spartan 3A by Xilinx. This gives flexibility for quick testing of the different solutions.

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II. Structural Diagram of the All Digital Phase Locked Loop

The structural diagram of the test setup is represented on Fig. 1 [1]:

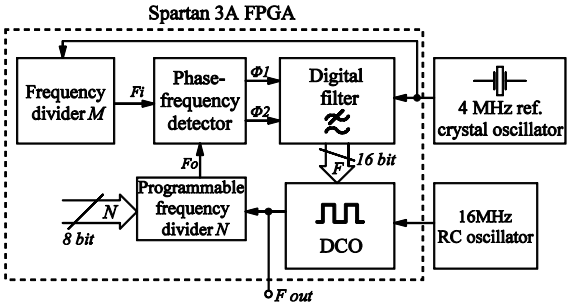

Fig. 1. Structural diagram of the test setup

A development board with FPGA programmable device Spartan 3A by Xilinx is used. It has USB interface for configuration of the FPGA and for power supply. It also has 4 capacitive touch sensitive buttons, 16 *MHz* RC oscillator and expansion connectors. An expansion board with 4 *MHz* quartz oscillator is developed for the different circuits analysis [1]. A digital USB oscilloscope Velleman PCSU1000 is used for examination of most of the proposed circuits and tasks. The basic block diagram of the developed PLL is drawn inside the FPGA chip.

III. Phase Frequency Detectors

There are different types of phase detectors. Their main differences are the width of the linear region in the phase response, and the frequency difference sensitivity. The detectors which are sensitive to the difference of the frequencies of the input signals are called phase-frequency detectors [2]. The other difference is the triggering event. The simplest phase detectors are insensitive to the difference in the frequencies of the input signals and are level triggered. These are called type 1 detectors. The input signals should be square wave and with the same 50% duty cycle [2]. Their linear range of the phase response is relatively narrow and repeats periodically. These detectors are used in PLL systems with narrow frequency range due to the risk of synchronization on multiple of the reference frequency. These types of detectors are most commonly built with an exclusive OR gate (XOR). The logical diagram with the timing diagrams and the phase response are represented on Fig. 2 [2]. The output of the

detector Φ is connected to an analog filter for demonstration of the phase response.

The schematic diagram of the detector with the analog filter is represented in *a*. The timing diagrams of the input signals and the Φ signal is represented in *b*. The phase response is represented in the form of voltage after the analog filter in *c*.

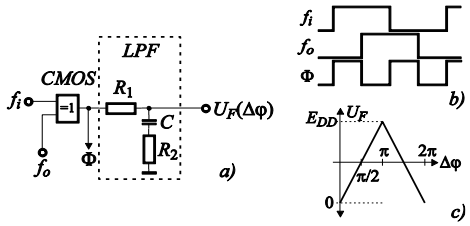

Fig. 2. XOR phase detector with LPF

As it can be seen from the diagrams the output frequency is twice the frequencies of the input signals. The phase response is with triangular shape and linear region from 0 to π. In order to work in the middle of the linear range the phase difference between the input signals should be π/2. In case of input signal loss, the detector works in the middle of the linear region [2].

The next type of phase detectors are edge triggered. These are also called type 2 detectors. In this type of detectors, the duty cycle of the input signals does not need to be 50% [3]. Its logical diagram along with the timing diagrams and the phase response is represented on Fig. 3:

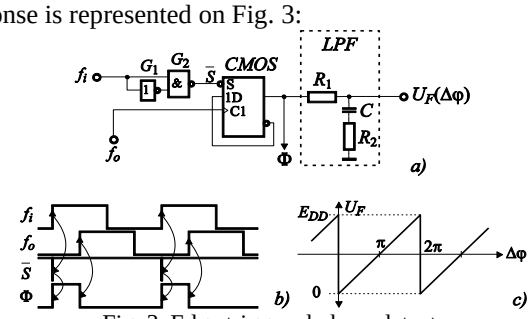

Fig. 3. Edge triggered phase detector

The triggering event in this detector is the rising edge of the input signals. The f_i signal is applied to a forming circuit which generates a short negative pulse after each rising edge of the signal [3]. This pulse sets the flip-flop. The f_o signal is applied to the clock input of the flip-flop and resets it when the rising edge arrives. As it can be seen from the timing diagrams the output frequency Φ is equal to the frequency of the input signals. The phase response is with sawtooth form and linear region from 0 to 2π. To work in the middle of the phase response, the steady phase difference between the input signals should be π. If the input signal f_i is lost the detector works in the middle of the linear region of the phase response.

The most serious drawback of these two-phase detectors is the relatively narrow linear range of the phase response. This leads to a worse interference immunity as the interference injected to the input of the detector can easily get the phase difference outside of the linear region [4].

The more advanced phase detectors are sensitive to the frequency difference of the input signals.

In their phase response there is a constant component outside of the linear range [2]. This gives the ability to tell which one of the input frequencies is higher. These detectors are used in PLL systems with wider working frequency range. On the startup the detector gives information what is the difference of the two frequencies and the proper code for the DCO synchronization is generated. These detectors are having the widest linear range in the phase response. The logical diagram of such detector is represented on Fig. 4. Its output signals are connected to a charge pump and a passive integrator for demonstration of the phase response [5].

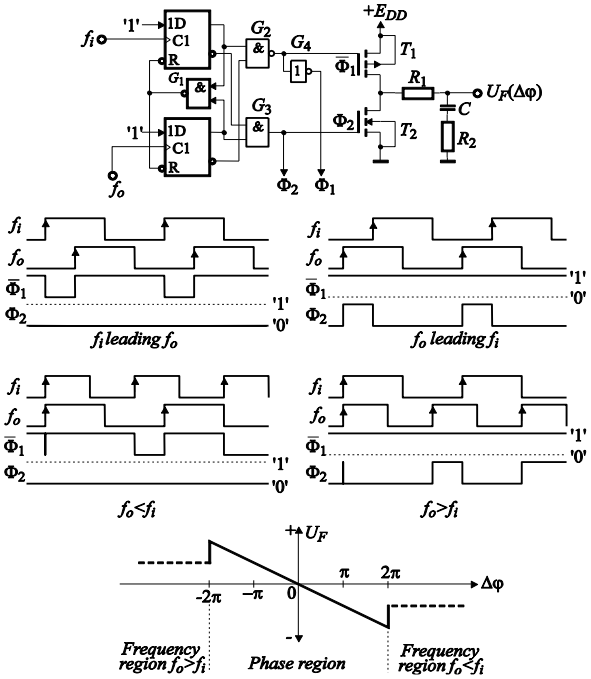

Fig. 4. Edge triggered phase-frequency detector

The compared signals f_i and f_o set on their rising edge two D-type flip-flops. The logical element NAND (G1) generates low level when both of the flip-flops are in set condition. This low level resets the flip-flops simultaneously. The output of the first flip-flop (Φ1 signal) is in high state if f_o leads f_i. The duration of the high state is equal to the duration between the rising edges of the two signals. If the f_i signal leads f_o the output of the second flip-flop (Φ2 signal) is high for the time difference between the rising edges. In the diagram there is shown a schematic of a charge pump and integrator for the demonstration purposes of the phase response. The detector has linear range of the phase response form -2π to 2π. In order to work in the middle of the linear range the phase difference between the input signals should be 0.

IV. Digitally Controlled Oscillators

In the analog PLL a main block is the Voltage Controlled Oscillator (VCO). It receives analog voltage and changes its output frequency depending on that voltage.

It has good parameters, but its price is high and in most of the cases it takes too much space on the Printed Circuit Board (PCB). It is also difficult for integration due to the large inductor on the chip [7]. For that reason, in the all-digital PLLs it is replaced by Digitally Controlled Oscillator. In it, the output frequency is controlled by a binary code. This

function can be achieved by several different methods. The first method is connecting a Digital to Analog Converter to a standard Voltage Controlled Oscillator [2]. It is not very desirable because we keep the high price and the difficulty for integration of the standard VCO. The advantage of the method is the easily controlled frequency step. The other more desirable and frequently used solution in the digital PLL is the high frequency square wave oscillator followed by a programmable frequency divider Fig. 5. It has the advantages of easy integration, lower price and higher stability. The disadvantage is the relatively high frequency of the oscillator required for a small enough frequency step. This leads to higher energy consumption.

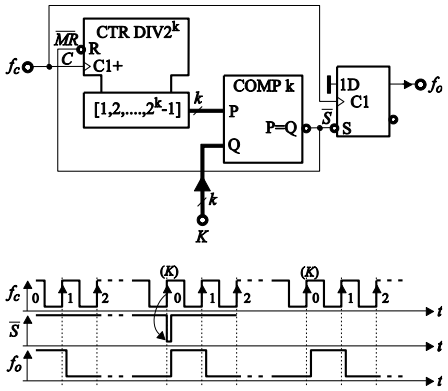

Fig. 5. Programmable frequency divider

The main problem of the concept is the increase of the frequency step when lowering the division coefficient *K*. A way to correct this is to connect a fixed frequency divider before the programmable one [8].

V. Digital Integrators and Filters

In the all-digital PLLs are used the same phase comparators as in the analog systems. The difference is that the analog filter or integrator is replaced with digital integrator or filter. This way the digital control code for the DCO is generated. Here the main logical diagrams and concepts will be discussed. The most common method for converting the time signals at the output of the phase detector to code is with digital integrator. The logical diagram of the integrator is represented on Fig. 6.

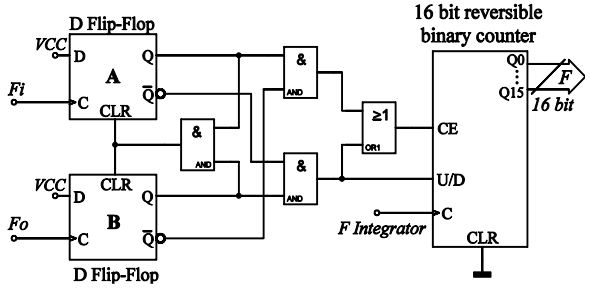

Fig. 6. Phase-frequency detector with digital integrator

It is built with a reversible counter with Clock Enable input and an Up/Down input. The clock frequency applied to the counter *F Integrator* is the equivalent of the time constant of the integrator.

By changing that frequency, the time constant can be changed. The outputs of the phase frequency detector are connected to the Count Enable and the Up/Down inputs of the counter. This way the integrator accumulates n pulses of *F Integrator* the time between the rising edges of the compared signals. The direction of accumulation is determined on which of the signals is leading. This way at the output of the counter is formed a digital code for the DCO [9].

Another version for conversion of the output signal of the phase detector Φ to digital code is proposed on Fig. 7:

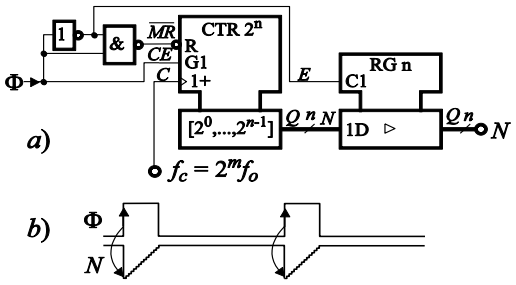

Fig. 7. Time-to-digital converter with parallel register

On the rising edge of the signal Φ the counter is being cleared and enabled and starts counting the pulses of the clock frequency f_c. On the falling edge of the signal the counter is disabled and stops counting [10].The accumulated value is stored to the parallel register after it [2]. This way the control code for the DCO is formed based on the phase difference of the signals. The main difference from the digital integrator is that the value of the counter here is cleared before each counting cycle. That means that in this case there is a fixed relation between time difference and digital code.

In some cases, for the stable operation of the PLL it is required additional filtration of the digital signal before applying to the DCO. It is possible to implement a standard Finite Impulse Response (FIR) filter into the FPGA Fig. 8 [2]:

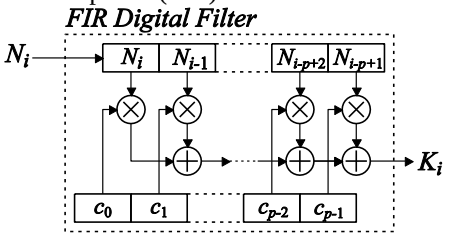

Fig. 8. Digital FIR filter

The logical diagram of the filter consists of a parallel shift register *N* for the samples from the digital integrator or filter. When a new sample enters the register from the left, all the samples inside are shifted with one position to the right. Every sample is multiplied by the corresponding coefficient *c* and the results are summed in order to form the current output sample K_i which is applied to the DCO [6]. One of the common realizations of the principle is the pipelined architecture Fig. 9. The circuit consists of *p* parallel registers connected in series forming one shift register. Before entering the register, the value N_i is divided by *p* into the DIV block.

The N_{i-p}/p sample is subtracted from the current filtered value K_{i-1} into the SUB block. At its output the value $K_{i-1} - N_{i-p}/p$ is formed. The value N_i/p is added to it into the SUM

block. The current sample of the output filtered signal $K_i = K_{i-1} - N_{i-p}/p + N_i/p$ is stored into the output parallel register.

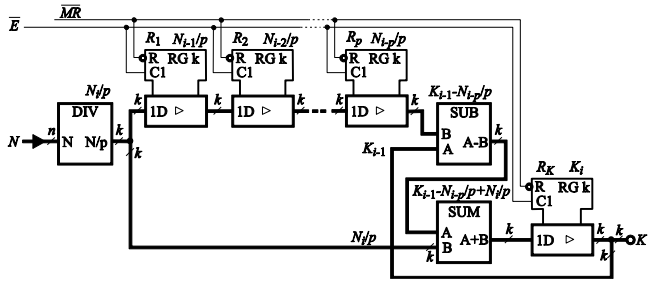

Fig. 9. Digital FIR filter with pipelined architecture

The division of the input samples is easily obtained if the division coefficient p is a power of two. The input sample is just shifted p bits toward the lower significant bits while the more significant bits are loaded with zeroes Fig. 10:

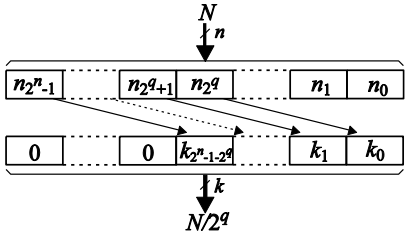

Fig. 10. Division by 2^q coefficient

The impulse response and the amplitude-frequency response of the filter with $p = 16$ is shown on Fig. 11:

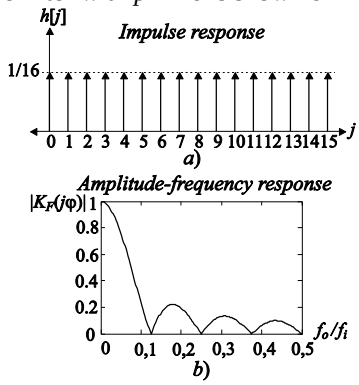

Fig. 11. Impulse and amplitude-frequency response of the filter

VI. Tasks for the Training

Several different tasks are developed for the education on all digital PLL:

- A digital PLL is built with phase comparator with XOR gate followed by digital integrator. The digital code from the integrator is applied to the DCO built with a programmable frequency divider. The circuit is tested with the digital oscilloscope, and the starting frequency of the DCO from which a successful synchronization is achieved is examined. The stability of the generated signal is observed, and the results are discussed.

- In the PLL from the previous task the phase detector is replaced with the phase-frequency detector from Fig. 7. The starting frequency of the DCO from which a quick synchronization is achieved is tested. The stability of the generated signal is observed. The results are discussed.

- To the PLL is added the digital FIR filter from Fig. 9. The system is tested for different values of multiplication of the reference frequency. The stability of the generated signal is observed with the digital oscilloscope. The time for synchronization for different frequencies is observed. The results are discussed.

VII. Conclusion

The developed digital functional equivalent modules for PLL give the students the opportunity to build all digital Phase Locked Loop on programmable logic device. The developed tasks offer the students the ability to design several different PLL topologies and to compare the performance of the different concepts. This way they can gain the knowledge on the PLL basics with the role of every block for the different PLL final parameters.

The use of FPGA programmable logic device gives the opportunity for every student to test a different circuit combination and even personal ideas for circuit improvements.

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