Design and Realization of Interleaved PFC Converter with GaN FETs and SiC Diodes

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Abstract – **This paper presents the straightforward design of interleaved Power Factor Correction converter using the Gallium Nitride transistors and Silicon Carbide diodes. The operating principles are briefly explained, including the simplified schematics. The prototype has been built and tested through lab measurements to verify the design. Experimental results are presented to support theoretical analysis and to demonstrate the converter performance. The goal was to demonstrate the capabilities of GaN transistors and SiC diodes in the high power applications.**

Keywords – **Boost, efficiency, GaN, interleaved, PFC, SiC.**

I. Introduction

Most off-line power supplies have a front end section made by a rectification bridge and a filter capacitor. Such power supply draws a current pulse during a small fraction of the each half-cycle duration. Pulsed current waveform produce non efficient RMS currents affecting the real power available from the mains [1]. In order to utilize the full line power and to reduce line current harmonics Power Factor Correction (PFC) circuits are required. The most popular PFC converter is a boost converter (Fig. 1). Mostly because the boost converter can have continuous input current that can be modulated with average current mode control to force the input current to track changes in the line voltage.

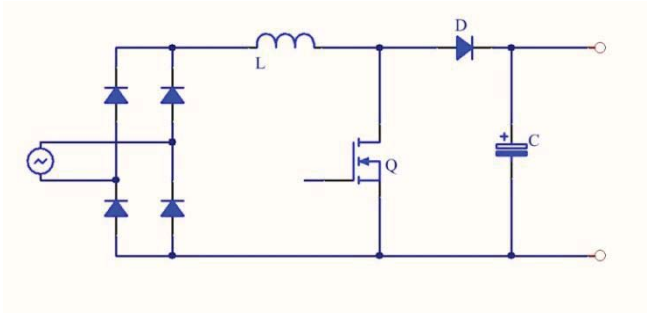

Fig. 1. PFC converter

II. Interleaved PFC Converter

The two phase interleaved PFC converter shown in Fig. 2 is practically made from two boost converters (phases) operating at the same frequency but 180° out of phase [2,3].

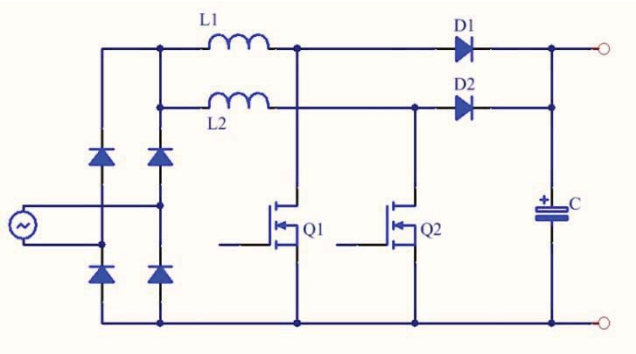

Fig. 2. Interleaved PFC converter

The input current is the sum of the two inductor currents. These currents are out of phase and tend to cancel each other, reducing the input ripple current caused by the boost inductors. The output bulk capacitor current is the sum of the two diode currents reduced by the load current. As a result of interleaving its RMS value is reduced and the size of the bulk capacitor is also reduced. By splitting the current into two paths, the conduction losses of power switches Q_1 and Q_2 and inductors L_1 and L_2 are reduced. The inductors magnetic volume is lower, because the energy storage requirement of the two interleaved inductors is two times smaller relative to the single inductor. The performances are improved at the cost of additional power switches, inductors and output diodes.

III. Design and Analysis

To design 1200W interleaved PFC converter we will start from the design specifications given in Table I.

TABLE I
DESIGN SPECIFICATIONS

		Min	Typ	Max	
Input voltage (AC)	V_{IN}	173	220	265	V
Output voltage	V_O		400		V
Output current	I_O		3		A
Output current limit	I_{OCL}		3.3		A
Full load efficiency	η	96			%
Switching frequency	f_{SW}		100		kHz

Converters duty cycle at the peak at low line operation is given by

$$D = \frac{V_{OUT} - V_{IN\_MIN} * \sqrt{2}}{V_{OUT}}$$

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Ripple current cancelation – ratio of input current to inductor ripple current at the peak at low line operation is

$$K = \frac{\Delta I_{IN}}{\Delta I_{L1}} = \frac{1 - 2 * D}{1 - D}$$

Inductor ripple current at the peak at low line operation can be calculated as

$$\Delta I_L = \frac{P_{OUT}\sqrt{2} * 0.3}{V_{IN\_MIN} * \eta * K}$$

Minimum inductance of the boost inductors is

$$L_{1\_MIN} = L_{2\_MIN} = \frac{V_{IN\_MIN} * \sqrt{2} * D}{\Delta I_L * f_{SW}}$$

Peak current of FETs and boost diodes is

$$I_{PK} = \left(\frac{P_{OUT} * \sqrt{2}}{2V_{IN_{MIN}} * \eta} + \frac{\Delta I_L}{2}\right) * 1.2$$

RMS current of FETs is determined by

$$I_{RMS} = \frac{P_{OUT}}{2 * \eta * V_{IN\_MIN} * \sqrt{2}} * \sqrt{2 - \frac{16 * V_{IN_{MIN}} * \sqrt{2}}{3 * \pi * V_{OUT}}}$$

Diodes average current is determined by

$$I_D = \frac{P_{OUT}}{2 * V_{OUT}}$$

Calculated values of the basic parameters of the each phase are given in Table II.

TABLE II
BASIC PARAMETERS OF THE EACH PHASE

		Max	Typ	Min	
Duty cycle	D			0.37	
Inductor ripple current	I_{PP}	7.88			A
Inductor RMS current	I_{LRMS}	4.23			A
Inductance	L			120	µH
FET RMS current	I_{RMS}	2.58			A
FET peak current	I_{PK}	11.12			A
Diode average current	I_{DAVG}	1.53			A
Diode peak current	I_{DPK}	11.12			A

As a power switch we will choose between a 650V MOSFET IPW65R095C7 and GaN FET TPH3205WSB [4] whose characteristics are given in Table III. GaN FET obviously has a better figure of merit (FOM) defined as

$$FOM = (Q_{GD} + Q_{GS}) * R_{DS}$$

The reverse recovery charge causes the boost diode to look like a short to the FET until the charge is cleared from the diode. This is a large source of switching loss in the PFC pre-converter. Those losses are dependent on the peak operating current and diode temperature. A silicon carbide diode C3D08065I [5] is chosen because it has no reverse recovery charge and therefore zero reverse recovery losses.

TABLE III
POWER SWITCH CHARACTERISTICS

	Q_{GD}	Q_{GS}	C_{OSS}	R_{DS}	FOM
IPW65R095C7	15nC	12nC	33pF	84mΩ	2268
TPH3205WSB	6nC	10nC	135pF	49mΩ	784

The output capacitor is selected based on holdup requirements and can be calculated as

$$C_{OUT} \geq \frac{2 * P_{OUT}}{f_{LINE}[(V_{OUT})^2 - (0.65 * V_{OUT})^2]}$$

IV. REALIZATION

The interleaved PFC converter has been realized on two layer FR-4 substrate, with a thickness of 1.6mm and 70µm copper with footprint 165 x 140mm. The boost inductors are wounded on two stacked iron powder toroids. Low side driver UCC27511 is used. The output capacitor is made of three 270µF electrolytic capacitors. Using isolation mains transformer and high power resistive load we have measured efficiency, power factor and also recorded the waveforms at the point of interest. Efficiency is over 98%, for 20 to 100% of the output power (Fig. 3). The power factor is presented in Fig. 4. Rectified line voltage and drain voltages are given in Fig. 5. and Fig. 6. Gate and drain voltage of the GaN FET are given in Fig. 7. Input line current with the respect to the line voltage is given in Fig. 8. Limited inrush current is recorded in Fig. 9. Output line ripple is given in Fig. 10. Output voltage startup into full load is given in Fig. 11. The converter prototype with top heatsink removed is presented in Fig.12. Finaly, the experimental setup in the lab is given in Fig. 13.

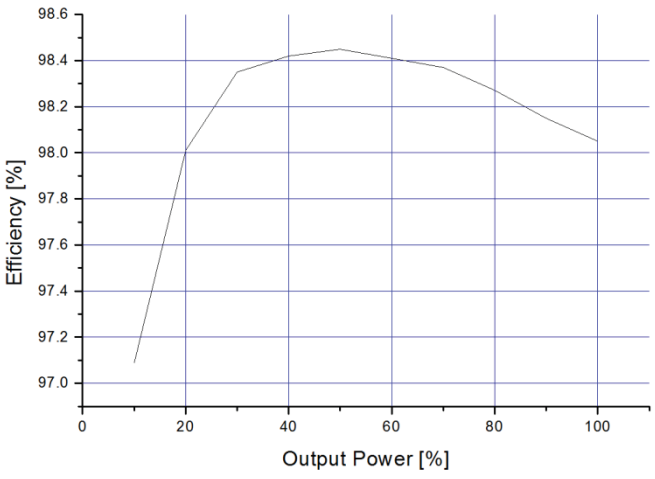

Fig. 3. Efficiency at 220V input

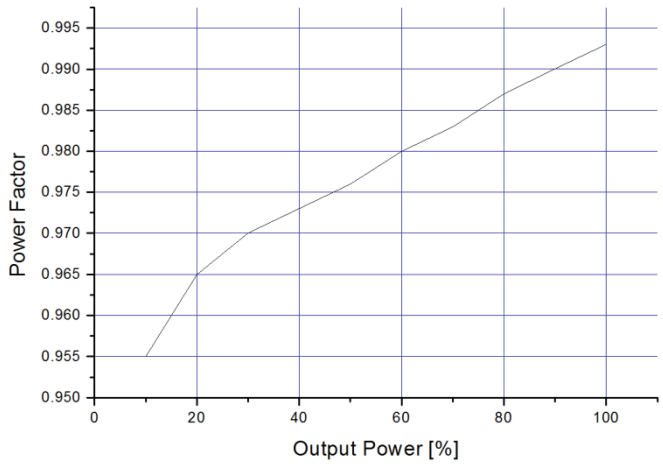

Fig. 4. Power factor

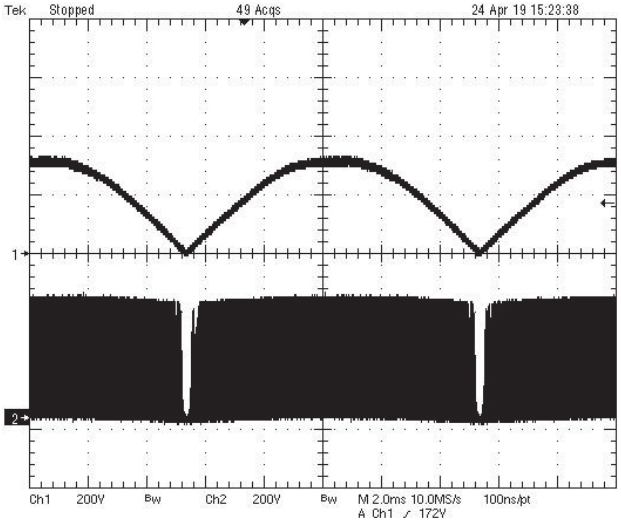

Fig. 5. Rectified line voltage and drain voltage

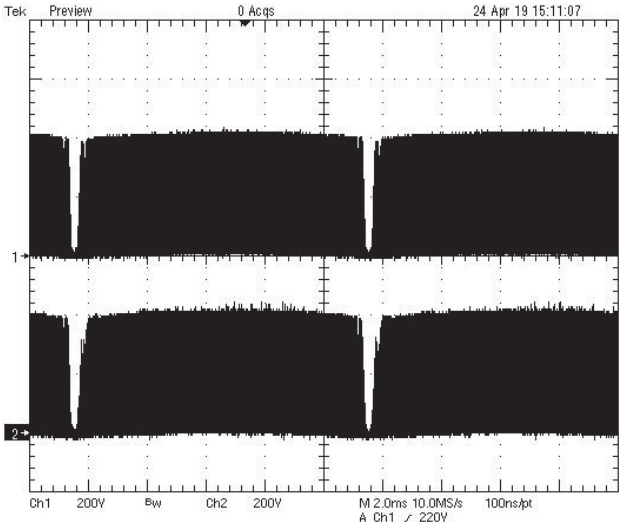

Fig. 6. Drain voltage simetry

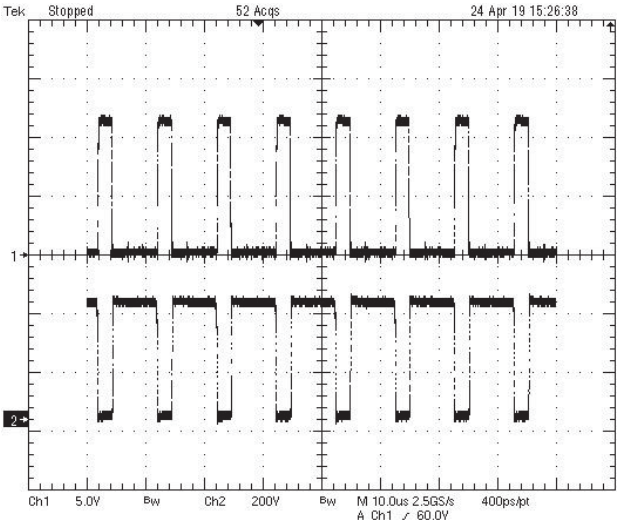

Fig. 7. Gate and drain voltage

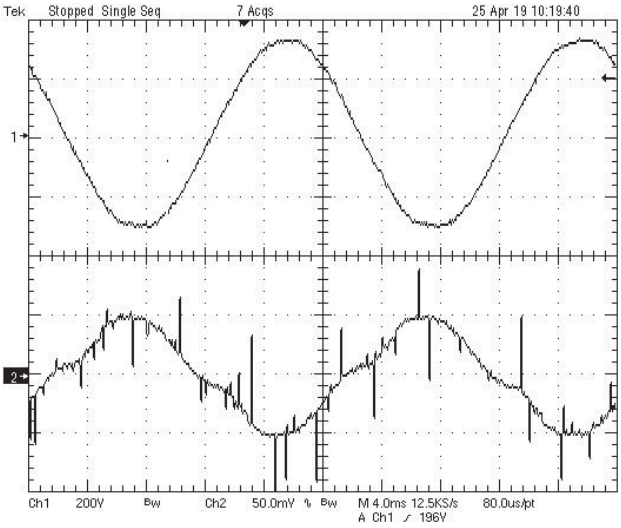

Fig. 8. Input line current

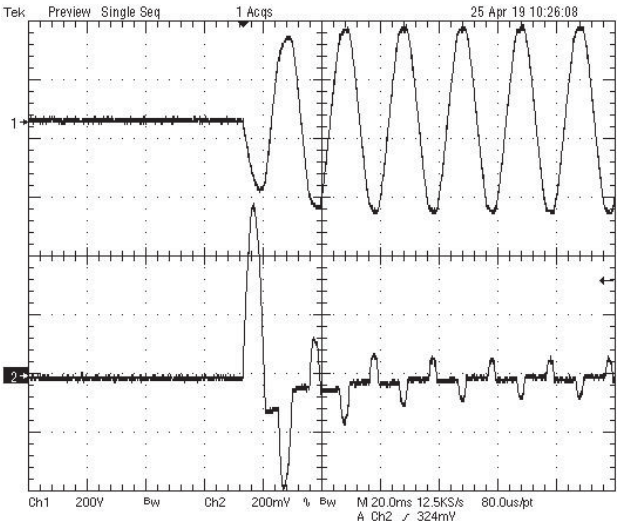

Fig. 9. Inrush current

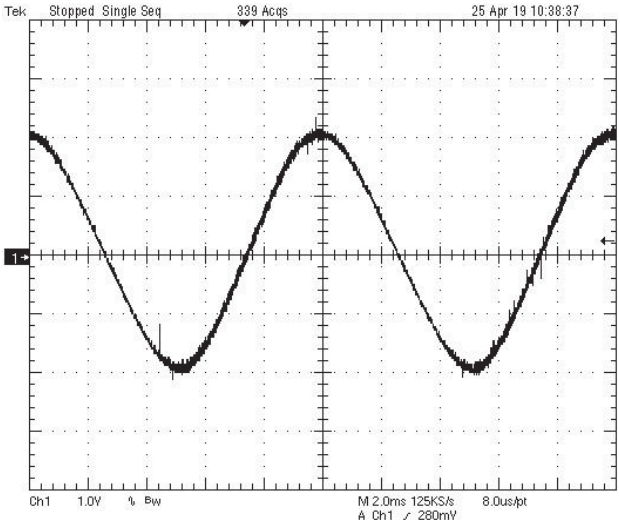

Fig. 10. Output ripple

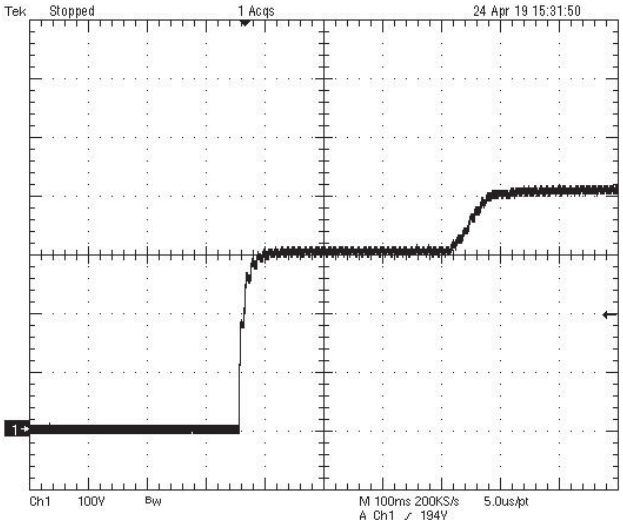

Fig. 11. Output voltage start up into full load

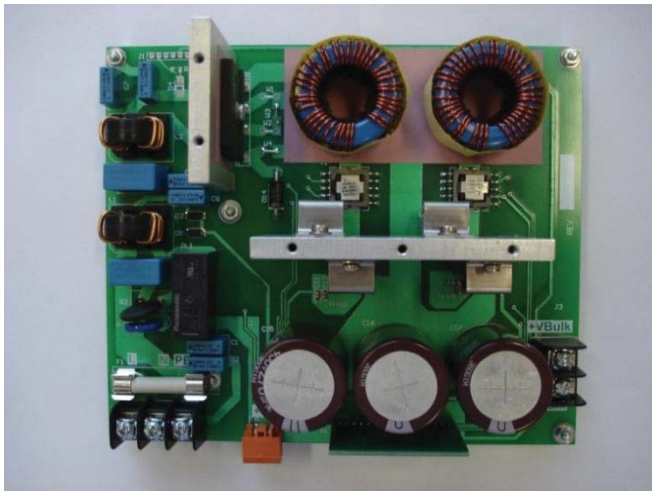

Fig. 12. The converter prototype

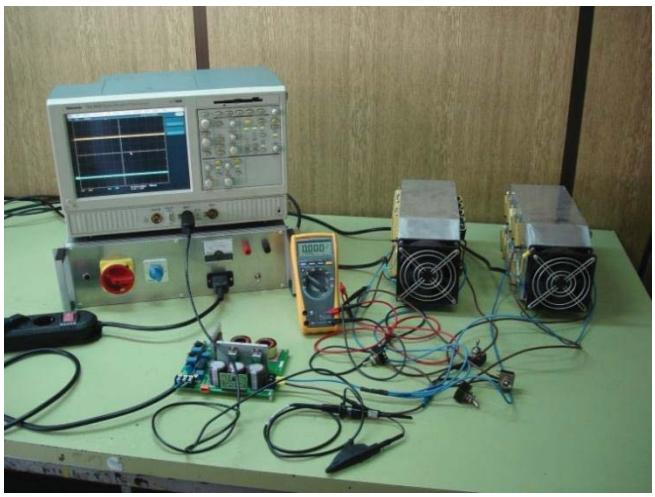

Fig. 13. Experimental setup in the lab

V. CONCLUSIONS

In this paper the design and realization of a two phase interleaved PFC converter with GaN FETs and SiC diodes is presented. Calculations and experimental results are presented. The prototype was built and tested. The results verified that the efficiency can go over 98%. Further increase in efficiency is possible by switching to Bridgeless PFC converter topology [6], in order to eliminate the losses of the rectification bridge.

ACKNOWLEDGEMENT

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