Increasing the Efficiency of Thyristor Spice Macromodels

Tsvetana G. Grigorova[1], Elissaveta D. Gadjeva[2], Katya K. Stefanova[3]

Abstract – **In this paper an approach is proposed for efficiency increasing of thyristor *Spice* macromodels. Taking into account the specificy of the modified nodal analysis, equivalent transformations of the standard thyristor library *Spice* macromodels are performed leading to the decreased size of the circuit matrix, thus accelerating the simulation. The computational time and the matrix size of the developed macromodels are investigated. Comparison of the simulation results for the transformed and for the original macromodel is realised using test examples.**

Keywords – **thyristor models, modified nodal analysis, *Spice* macromodels, behavioral modeling**

I. INTRODUCTION

Power electronics is of great importance for the electronic systems ranging from wireless communication devices, portable and desktop computers, to telecommunication infrastructure, and industrial systems. The enhanced development of power electronics technology imposes the necessity of effective computational tools for computer-aided analysis and design. Recently, simulation methods and program tools are of significant importance for the designers involved in the power electronics area dealing with the convertion and switching of electrical energy for power applications [1,2,3]. The electrical simulation of the power convertor circuits is proved to be useful tool for analysis of circuit behaviour and for investigating the critical operation conditions of power semiconductor devices. It allows also the user to take into consideration the circuit parasitic elements and effects which often play a dominant role.

The general-purpose circuit analysis programs such as *OrCAD PSpice* [4,5] are successfully used for analysis and design of power electronic circuits. The *PSpice*-like simulators provide component macromodels of power control circuits, represented as subcircuits in the model libraries.

The investigation of power electronic circuits in the time domain sets specific requirements to the simulation algorithms: fast simulation, accuracy control and convergence. In this respect, it is very important to develop device macromodels meeting these contradictory requirements.

In the present paper an improved *Spice* thyristor macromodel is developed, which leads to increasing the effectiveness of the standard circuit simulation *PSpice*-like programs.

II. MODIFIED THYRISTOR MACROMODEL

The representation of the circuit elements in the circuit matrix using the modified nodal analysis (MNA) is used for substantiation of the macromodels. The MNA is widely used in contemporary circut simulators to introduce a variety of circuit components in the matrix, which do not have an admittance representation [6]. Using this approach, the component equations of these “unsuitable” elements are added to the nodal equations. As a result, the circut matrix is expanded as shown in Fig. 1. Such an element is the voltage controlled voltage source (VCVS), which is often used in behavoiral thyristor macromodels to define inner model variables. The component equation of the VCVS has the form [6]:

$$V_{st} = \mu V_{pq} \tag{1}$$

or

$$V_s - V_t - \mu V_p + \mu V_q = 0 \tag{2}$$

The inclusion of the VCVS in the circuit matrix is presented in Fig. 2. A a result, the circuit matrix size n is increased by $\Delta n = 1$.

The standard thyristor *PSpice* macromodel shown in Fig. 3, is based on VCVS of **ETABLE** type, which combines VCVS of **EVALUE** type and a limiter element. The variables, introduced in the Q_1 block of the standard *PSpice* thyristor behavioral macromodel, are defined by VCVS as shown in Fig. 4a. The role of the resistor R_{mod} is to meet the require-

$$\begin{array}{|c|c|}\hline \mathbf{Y} & \mathbf{A}_2 \\ \hline \mathbf{A}_1 & \mathbf{Z} \\ \hline \end{array} \cdot \begin{array}{|c|}\hline \mathbf{U} \\ \hline \mathbf{I} \\ \hline \end{array} = \begin{array}{|c|}\hline \mathbf{J} \\ \hline \mathbf{E} \\ \hline \end{array}$$

Fig. 1. Structure of the circuit matrix using modified nodal analysis

$$\begin{array}{c|c|c|c|c|c|c|c|c|c|} & & s & & t & & p & & q & n+1 \\ \hline & & & & & & & & & \\ \hline s & & & & & & & & & 1 \\ \hline & & & & & & & & & \\ \hline t & & & & & & & & & -1 \\ \hline & & & & & & & & & \\ \hline n+1 & & 1 & & -1 & & -\mu & & \mu & \\ \hline \end{array} \cdot \begin{array}{|c|}\hline \\ \\ \mathbf{U} \\ \\ \\ \hline I_e \\ \hline \end{array} = \begin{array}{|c|}\hline \\ \\ \mathbf{J} \\ \\ \\ \hline 0 \\ \hline \end{array}$$

Fig. 2. The inclusion of the VCVS in the circuit matrix

---

[1] Tsvetana G. Grigorova is with the Faculty of Electronics and Automatic, Technical University of Sofia, Branch Plovdiv, boul. “Sankt Peterburg” 61, 400 Plovdiv, Bulgaria, E-mail:grigorova@hotmail.com

[2] Elissaveta D. Gadjeva is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, kv. Darvenitsa, bl. 1, 1756 Sofia, Bulgaria, E-mail: egadjeva@vmei.acad.bg

[3] Katya K. Stefanova is with the Technical College “John Atanasov”, “Br. Bakston” Str. 71A, Plovdiv, E-mail: k_stefanova@yahoo.com

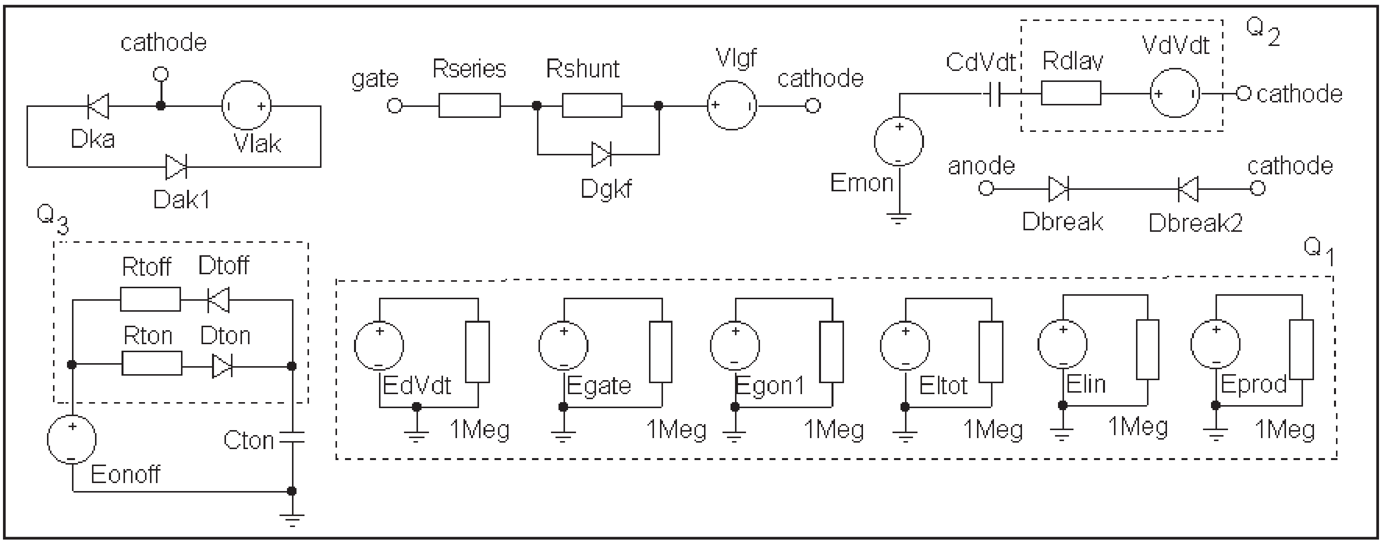
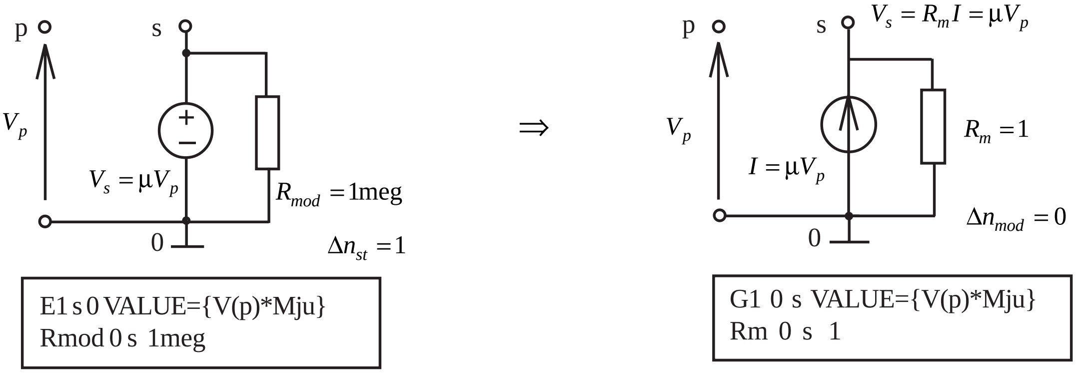


Fig. 3. The standard thyristor PSpice macromodel



```
E1 s 0 VALUE={V(p)*Mju}
Rmod 0 s  1meg
```

a)

```
G1 0 s VALUE={V(p)*Mju}
Rm 0 s 1
```

b)

Fig. 4. Transformation of VCVS to VCCS in the behavioral macromodel

ment of the *PSpice* simulator for a minimum two branches connected to a node. The circuit in Fig. 4a can be replaced by the circuit shown in Fig. 4b consisting of voltage controlled current source (VCCS) and a resistor R_m of value 1 Ω. The standard model in Fig. 4a increases the matrix order by $\Delta n_{st}=1$. The modified model using VCCS (Fig. 4b) has admittance description and it does not expand the circuit matrix ($\Delta n_{mod}=0$). The effectiveness of the modified model is characterised by the difference $\Delta n=\Delta n_{st}-\Delta n_{mod}=1$.

According to Fig. 3, the elements *Eprod* and *Rprod* in the standard *PSpice* library model

```
Eprod  prod  0  TABLE {v(anode,cathode)*v(Itot)} (0 0) (1 1)
Rprod  prod  0   1meg
```

can be replaced by the elements *Gprod* and *Rprod* in the modified model in the form:

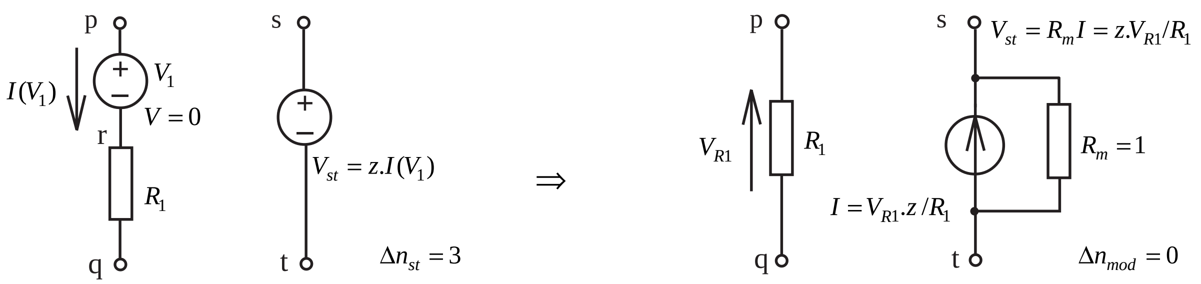
```
Gprod  0 prod TABLE {v(anode,cathode)*v(Itot)} (0 0) (1 1)
Rprod prod 0  1
```

In order to define the cirrent controlled voltage source (CCVS) $V_{st}=z.I(V_1)$ in the *PSpice* models, independent voltage source of value $V = 0$ is introduced to model the controlling branch. Such an element is used in the block Q_2 of the behaioral macromodel in Fig. 3.

The circuit of CCVS shown in Fig. 5a is characterised by $\Delta n_{st}=3$. It can be transformed equivalently in the circuit shown in Fig. 5b, which does not expand the circuit matrix ($\Delta n_{mod}=0$). The decreasing of the matrix order is defined by the difference $\Delta n=3$.

The diode group used in the block Q_3 of the standard thyristor behavioral macromodel (Fig. 3) is presented in Fig. 6a. It is characterized by $\Delta n_{st}=2$. It can be equivalently transformed combining the external resistance R_1 connected in series with the diode, and the resistance R_{s1} defined in the diode model. The resulting modified circut is shown in Fig. 6b, where the diode resistance is $R_s=R_{s1}+R_1$. It is characterised by $\Delta n_{mod}=1$.The decreasing of the matrix order is $\Delta n=1$.

Applying similar transformations, the modified thyristor model is obtained. The *PSpice* description of this model is shown in Fig. 7. The introduced modifications in the standard model are given in italic. As a result of these modifications, the matrix order of the obtained thyristor model decreases by $\Delta n=10$ for each thyristor element in comparison with the standard model.



```
V1  p  r  DC   0
R1   r  q  {R1}
E1 s  t VALUE= {z*I(V1)}
```

a)

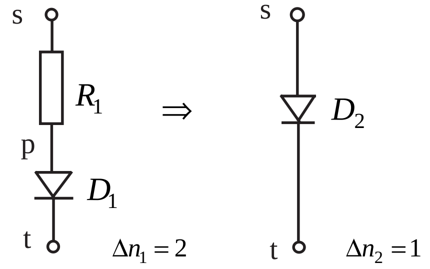
```
R1    p  q  {R1}
G1  t  s   VALUE= {z*V(p,q)/R1}
Rm   s  t  1
```

b)

Fig. 5. Transformation of CCVS to VCCS in the behavioral macromodel

```
.subckt Scr anode gate cathode PARAMS: Vdrm=1500v
+ Vrrm=1500v   Idrm=10u Ih=50ma  dVdt=1000e Igt=25ma
+ Vgt=1.5v Vtm=2v  Itm=150  Ton=1u  Toff=25u
Scr   anode   anode0  control  0   Vswitch
Dak1 anode0  anode2  Dakfwd  OFF
Dka  cathode anode0  Dkarev  OFF
VIak  anode2  cathode
Emon  dvdt0  0  TABLE {v(anode,cathode)} (0 0) (2000 2000)
CdVdt  dvdt0  dvdt1  100pfd
Rdlay  dvdt1   cathode   1k
GdVdt  0 condvdt   TABLE
+ {1e-3*v(dvdt1,cathode)-100p*dVdt}   (0  0 ) (.1m  10)
RdVdt   condvdt 0   1
Rseries  gate   gate1  {(Vgt-0.65)/Igt}
Rshunt   gate1   gate2   {0.65/Igt}
Dgkf   gate1  gate2  Dgk
VIgf   gate2  cathode
Ggate1   0 gate4    TABLE {i(Vigf)-0.95*Igt} (0 0)  (1m  10)
Rgate1 gate4  0   1
Ggon1   0 congate  TABLE
+ {v(gate4)*v(anode,cathode)}  (0  0)  (10  10)
Rgon1   congate  0    1
GItot    0    Itot    TABLE {i(VIak)+5E-5*i(VIgf)/Igt}
+    (0  0)  (2000  2000)
RItot    Itot   0    1
Gprod   0   prod   TABLE {v(anode,cathode)*v(Itot)}  (0  0)  (1  1)
Rprod   prod   0    1
Glin    0  conmain   TABLE
+      {10*(v(prod) - (Vtm*Ih))/(Vtm*Ih)}  (0  0)  (2  10)
Rlin    conmain 0  1
Eonoff  contot  0   TABLE
+   {v(congate)+v(conmain)+v(condvdt)}  (0 0)  (10 10)
Dton    contot    control Delaya
Dtoff  control  contot    Delayb
Cton   control 0   {Ton/454}
Dbreak  anode   break1  Dbreak
Dbreak2 cathode break1   Dseries
.MODEL Vswitch vswitch (Ron = {(Vtm-0.7)/Itm},
+  Roff = {Vdrm*Vdrm/(Vtm*Ih)}, Von = 5.0,  Voff = 3.5)
.MODEL  Dgk  D  (Is=1E-16 Cjo=50pf Rs=5)
.MODEL  Dseries D  (Is=1E-14)
.MODEL  Delay   D   (Is=1E-12 Cjo=5pf  Rs=0.01)
.MODEL   Delaya    D   (Is=1E-12  Cjo=5pf   Rs=825.01)
.MODEL    Delayb   D   (Is=1E-12  Cjo=5pf   Rs={290*Toff/Ton})
.MODEL  Dkarev  D  (Is=1E-10 Cjo=5pf  Rs=0.01)
.MODEL  Dakfwd  D  (Is=4E-11 Cjo=5pf)
.MODEL  Dbreak  D  (Ibv=1E-7 Bv={1.1*Vrrm} Cjo=5p Rs=0.5)
.Model D D(Rs=1m)
Rfloat  gate    cathode 1e10
.ends
```

Fig. 7. Description of the modified behavioral thyristor macromodel



```
Diode1    p   t     D1
R1  s  p  {R1}
.Model  D1   D (Rs={Rs1})
```

```
Diode1     s   t    D2
.Model  D2   D (Rs={Rs1+R1})
```

a)

b)

Fig. 6. Transformation of the diode circuit in the behavioral macromodel

III. EXAMPLE

Test circuits are simulated in order to investigate the model effectiveness. The matrix expansion and the simulation time are calculated.

The current-fed parallel inverter with voltage limitation shown in Fig. 8 is simulated in the time-domain using the standard and the modified thyristor macromodel. The obtained results for the voltage $V_{Rt}(t)$ are presented in Fig. 9. The standard and the modified thyristor macromodels are characterized by the same accuracy.

Circuits of different size are simulated to investigate the effectiveness of modified thyristor macromodel. The obtained results of the simulation in the time domain are presented in Table 1, where ν is the number of nodes of the circuit, n_{st} is the matrix order of the circuit using standard macromodel and n_{mod} is the matrix order of the circuit using the modified

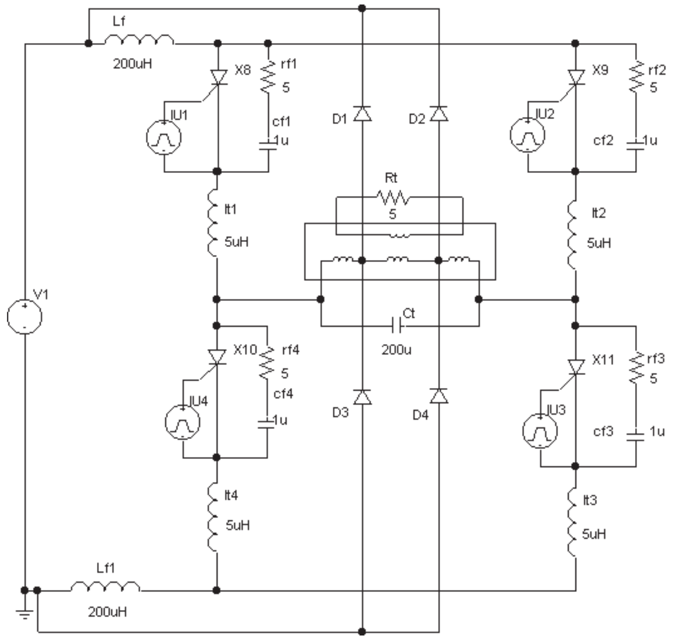


Fig. 8. The current-fed parallel inverter with voltage limitation

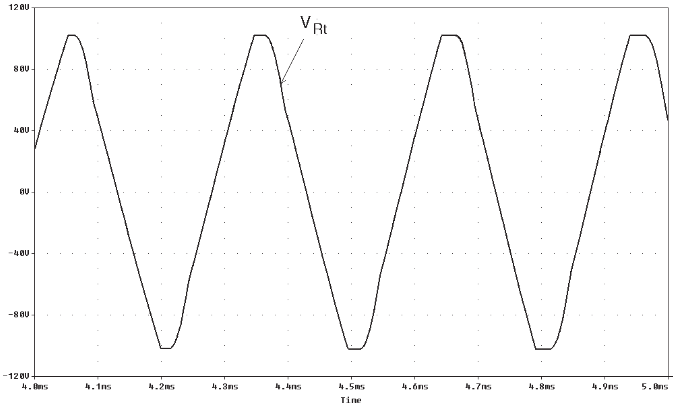


Fig. 9. Simulation results for the voltage $V_{Rt}(t)$ of the example circuit

macromodel. The dependence of the matrix order on the node number v is represented graphically in Fig. 10 and the dependence of the calculation time on the node number is shown in Fig. 11. The effectiveness of the modified macromodel is characterized by the acceleration of the simulation process:

$$\delta = \frac{100.(t_{st} - t_{mod})}{t_{st}} \%$$

Using the modified macromodel, the acceleration is 7% for $v = 100$ and reaches 16% for $v \geq 500$.

CONCLUSIONS

A marcomodel of higher efficiency of the library *PSpice* thyristor behavioral macromodel has been developed in the present work. The improved computational effectiveness is achieved by model size reduction. The possibilities of the input language of the *PSpice* simulator are used. The subcircuit description of the modified model in accordance with the *PSpice* input language is presented. Test examples are simulated to investigate the effectiveness dependence on the circuit node number .

TABLE 1 - Effectiveness assessment of thyristor model

ν	n_{st}	n_{mod}	t_{st} [s]	t_{mod} [s]
100	169	129	54.3	50.5
300	505	385	198	181
400	673	513	269.5	224
500	841	641	358	324
600	1009	769	448	374

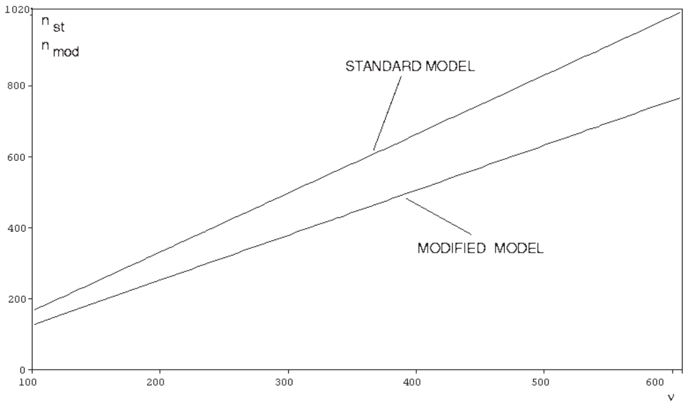


Fig. 10. Dependence of the matrix order on the node number

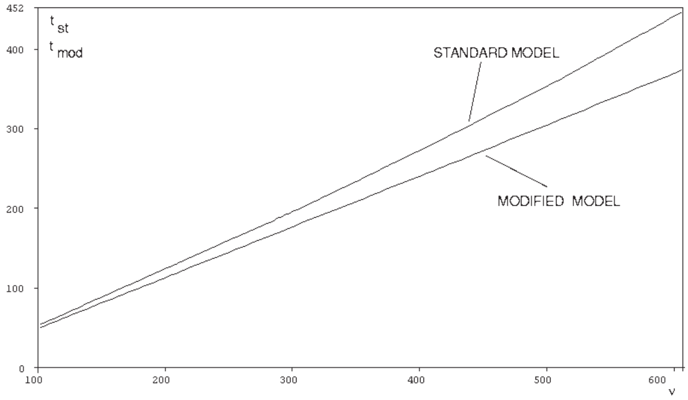


Fig. 11. Dependence of the calculation time on the node number

REFERENCES

[1] F. J. Gracia, F. Ariziti and F. J. Aranceta ”A nonideal macromodel of thyristor for transient analysis in power electronic systems”, IEEE Trans. Iind. Electron., vol.37, No 6, dec. 1990, pp. 514-520

[2] R. L. Avant and F.C. Lee, “A unified SCR model for continuous topology CADA”, IE-31, no.4, Nov.1984, pp.352-360

[3] A. Brambilla and E. Dallago “A circuit –level simulation model of PNPN devices”, IEEE Trans. Computer-aided design, vol.9, No.12, dec.1990, pp. 1254-1264.

[4] OrCAD PSpice A/D. Circuit Analysis Software. Reference Manual. OrCAD Inc., USA, 1998.

[5] OrCAD PSpice and Basics. Circuit Analysis Software. OrCAD Inc., USA, 1998.

[6] J. Vlach, K. Singhal, “Computer Methods for Circuit Analysis and Design”, VNB, N.Y. 1988.