Modeling of a selfoscillating control system of a transistor oscillator for tube welding using Spice

Georgi Tz. Kunov[1], Elissaveta D. Gadjeva[2], Ilian D. Eftov[3]

Abstract – **In this paper a selfoscillating control system of a bridge transistor oscillator is proposed with a parallel resonant circuit as a load, which technologycal application is the tube welding. The system is characterized by good dynamic characteristics allowing precise tracking of the fast changes in the technologycal process. A computer model of the control system is developed and simulated using the general-purpose circuit analysis program *OrCAD PSpice* and the simulation results are presented.**

Keywords **– selfoscillating control system, tube welding, computer simulation, Spice modeling**

I. Introduction

The development of the manufacturing technologies for power MOSFET transistors provides the possibility of producing power transistor oscillators, which are of a great practical importance.

The high-frequency tube welding is one particular application of the various induction technologies [1–6]. The sharp resonance frequency change of the parallel resonant circuit (the transistor oscillator load) in the starting moment of the welding process is an important specific feature of the induction tube welding technology.

The optimal mode of commutation of the transistors in the transistor oscillator takes place when their current is in the same phase with the voltage on the load resonant circuit.

The classical control providing this mode of operation, consists of a phase detector, with an output signal that changes the frequency of a voltage controlled oscillator (VCO) [2,3]. This system is characterized by a certain delay of the frequency tracking reaction due to the existence of filter elements in the feedback circuit.

In the present work a selfoscillating control system is developed which is significantly superior with respect to the speed to the control systems based on the classical principle. Such control systems have been proposed for thyristor oscillators [4,5].

[1]Georgi Tz. Kunov is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, kv. Darvenitsa, bl. 1, 1756 Sofia, Bulgaria, E-mail: gkunov@tu-sofia.acad.bg

[2]Elissaveta D. Gadjeva is with the Faculty of Electronic Engineering and Technologies, Technical University of Sofia, kv. Darvenitsa,bl.1,1756 Sofia, Bulgaria, E-mail: egadjeva@vmei.acad.bg

[3]Ilian D. Eftov is with Faculty of Electronic Engineering and Technologies, Technical University of Sofia, kv. Darvenitsa, bl. 1, 1756 Sofia, Bulgaria

II. Descripton of the Control System

A. Transistor oscillator

The full bridge transistor oscillator circuit is shown in Fig. 1. The L_2 element is the inductor inductance and the R_4 element is the equivalent active resistance of the welding seam. These elements, together with the capacitor C_4, form a parallel resonant circuit, which represents the oscillator load. The additional inductance element L_1 ensures the inductance character of the I_s current in the oscillator diagonal. The remaining resistors are auxiliarly elements needed to measure currents in the model of the *PSpice* simulator. The R_s resistor is a shunt resistor sensing the I_s current through the diagonal and the transistors. The R_4 resistor is a shunt resistor, giving information for the I_s current through the compensating capacitor C_4. The resistors R_1–R_3 form a resistor voltage divider thacking the load voltage U_c. By the so chosen virtual ground (GND) the I_s current is visualised by the *PSpice* simulator with a reversed phase according to the U_c voltage (Fig. 4a). In fact I_s and U_s are in phase. The IRFP460 transistor of the standard *PSpice* library PWRMOS.SLB is used for the transistors M_1, M_2, M_3 and M_4.

B. Control Selfoscillating System and Phase Correction System

The control selfoscillating system and the phase correction system are shown in Fig. 2.

The zero comparators S_1, S_2 and S_3 record the moments of subsequent of the positive and negative halfperiods of the corresponding signals U_c, I_c and I_s. The output values U_{s1}, U_{s2} and U_{s3} are shown in Fig 4b. The logical elements U_5, U_6, U_7 and U_8 realise the logical function *EXCLUSIVE OR*. The output values of the elements U_{u5} and U_{u6} are:

$$U_{u5} = U_c \oplus I_c$$
$$U_{u6} = \overline{U}_c \oplus I_c . \quad (1)$$

The logical values of 1 for the elements U_{u5} and U_{u6} commutate the current sources G_1 and G_2 in such a way that a linear increasing/decreasing voltage U_{so} is formed on the C_7 capacitor (Fig. 4c). U_{so} increases in the interval $0 \div 90^o$ and decreases in the interval $90^o \div 180^o$ of each positive and negative halfwave of the U_c voltage. The diode D_3 and the capacitor C_{10} realise the sample-and-hold function for the maximal value of the U_{so} voltage.

In order to ensure the condition I_s and U_c to be in phase, it

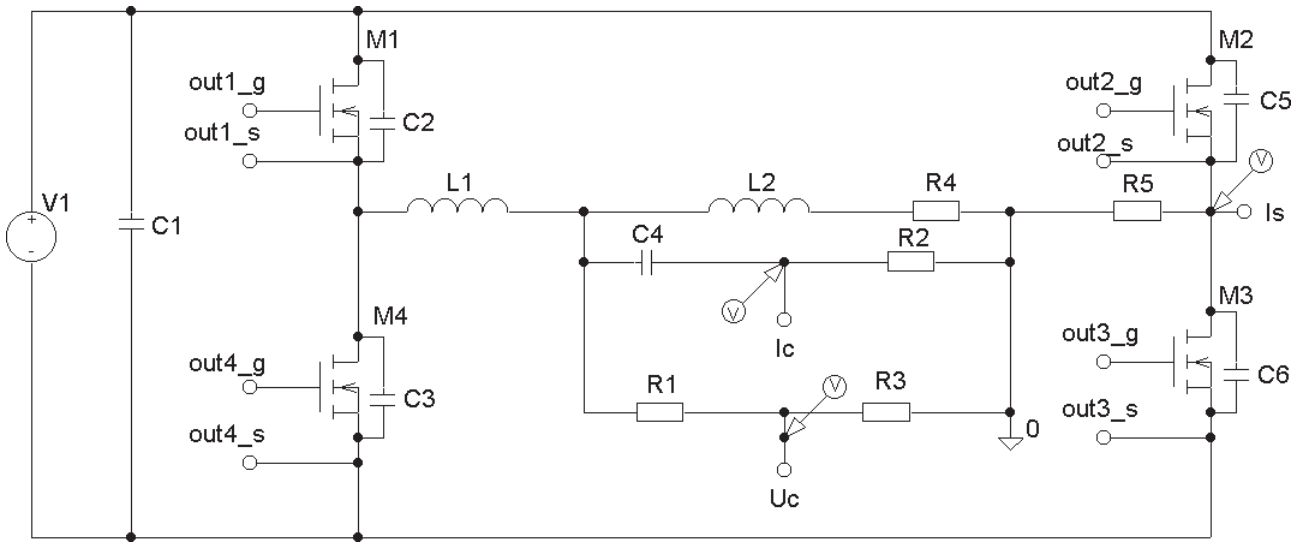

Fig. 1. Transistor oscillator

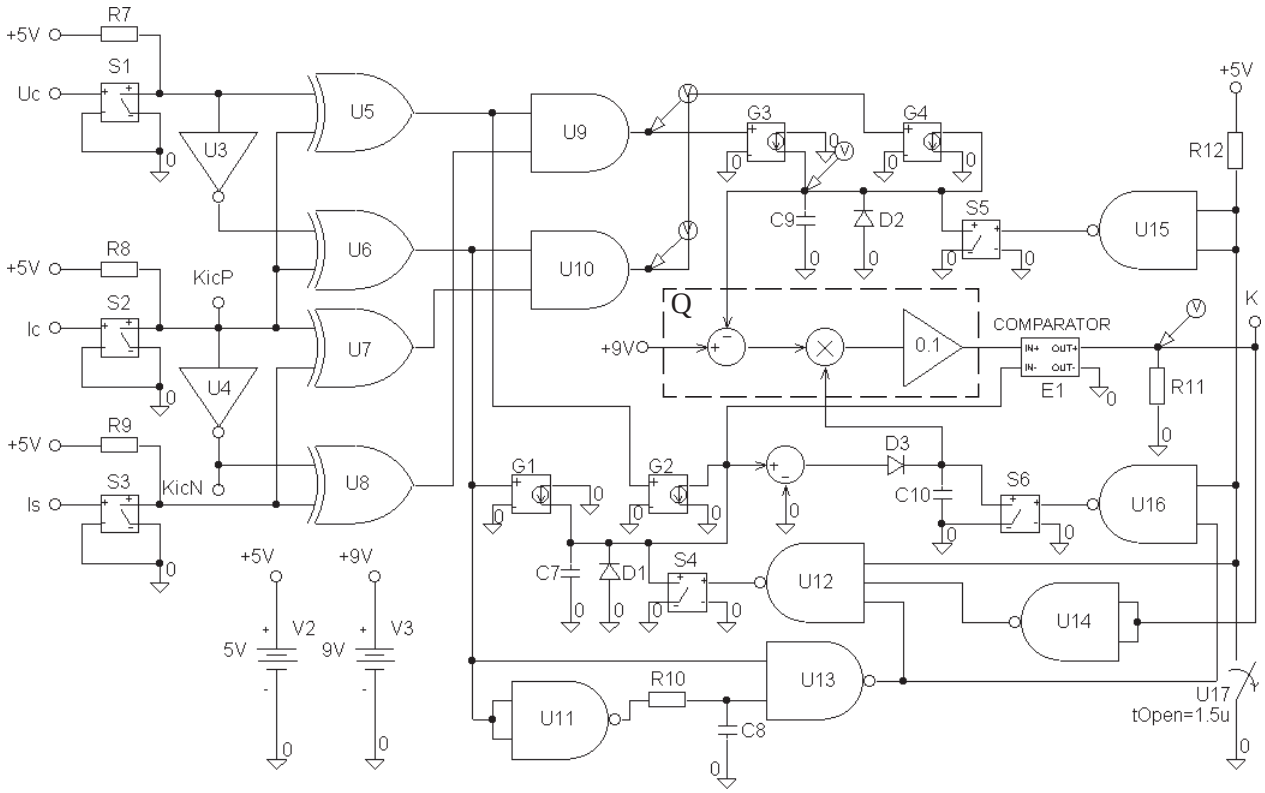

Fig. 2. Control selfoscillating system and phase correction system

is necessary to commutate the transistors M_1, M_3 and M_2, M_4 at the definite angle outrunning the sign change of the U_c halfwaves. A voltage U_φ proportional to this angle lead is formed on the capacitor C_9 using the current sources G_3 and G_4. The latter are controlled by the outputs of the logical circuits U_9 and U_{10}. They are presented in Fig. 4b as U_{u9} and U_{u10}. The corresponding logical values are as follows:

– for capacitive detuning of I_s with respect to U_c (a phase lead of I_s with respect to U_c):

$$U_{u9} = (U_c \oplus I_c) \& (\bar{I}_c \oplus I_s) = 1 \qquad (2)$$

– for inductive detuning of I_s with respect to U_c (a phase lead of U_c with respect to I_s):

$$U_{u10} = (\bar{U}_c \oplus I_c) \& (\bar{I}_c \oplus I_s) = 1 \qquad (3)$$

The signal U_{msh} represents the scaled signal U_{so} in the form:

$$U_{msh} = \frac{9V - U_\varphi}{10} \cdot U_{so} \qquad (4)$$

The signals U_{msh} and U_{so} are compared at the inputs IN^+ and IN^- of the comparator E_1. As a result, the signal U_k is

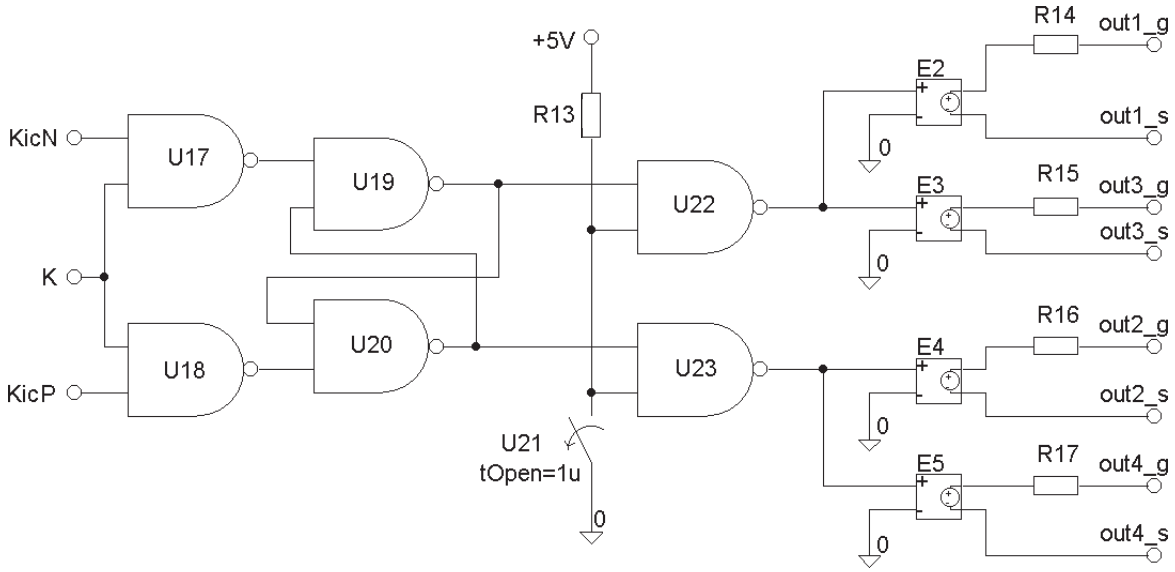

Fig. 3. Driver circuit

formed at the output of the comparator E_1. The leading edge of the U_k voltage defines the angle of the outrunning commutation of the transistors according to the sign change of the U_c voltage, when the current I_c is in phase with the U_c voltage.

The signal U_k is applied simultaneously to the logical elements U_{17} and U_{18} of the driver circuit (Fig. 3). Depending on the sign of the moment current value I_c , the logical element U_{17} or U_{18} is enabled. Passing through these elements, U_c changes the logical state of the RS-trigger U_{19}–U_{20}. In this way the working up to this moment transistor pair is switched off and the next transistor pair is switched on.

The logical elements U_{11} and U_{13} form short pulses in the sign change moment of the U_c voltage. They reset the sample-and-hold circuit. The reset of the U_{so} signal is performed by the U_k voltage.

III. PSpice Macromodeling of the Selfoscillating Control System and Phase Correction System

The developed control system is modeled as a mixed-type circuit and simulation in the time domain using *OrCAD PSpice* program is performed. Computer models at component level as well as analog behavioral models are built. A number of analog behavioral blocks of the system-level model library **ABM.lib** are used to model the subcircut shown in Fig. 2: voltage controlled switches of **S**-type, multipliers (**MULT**), gain blocks (**GAIN**), etc. The block *Q* is used to calculate the U_{msh} voltage in accordance with Eq. (3). The comparator circuit COMPARATOR is described using dependent voltage source of **EVALUE** type using the expression for the output voltage:

$$U_{out} = \begin{cases} 0 \text{ for } U_{in} \le 0 \\ 1 \text{ for } U_{in} > 0 \end{cases} \qquad (5)$$

The dependence (5) is defined by the expression

(SIGN(V(IN+,IN-)+1)/2.

in the EXPRESSION field of the **EVALUE** element.

IV. Conclusions

An improved solution for a selfoscillating control system with a bridge transistor oscillator has been developed. The control system corresponds to the specific features of the technologycal process of induction tube welding.

A computer mixed-type model of the system is developed for the control system using the rich possibilities of the *OrCAD PSpice* program. The simulation results of the time-domain analysis are presented.

References

[1] Dede, F. J., Esteve, V., Jordan, J., Gonzalez, J. V., Maset, F., On the Design and Control Strategy of High Power, High Frequency Convertors for Tube Welding Applications, The Pce-Yokohama Conference'93, Yokohama, Japan, April 1993.

[2] Frank, W. E., Der, C. E., Solid-State RF Generators for Induction Heating Applications, Society IEEE-IAS-Annual Meeting October 4-7, 1982, San Francisco, CA, pp. 939-944.

[3] Loveless, D. L., Cook, R. L., Rudnev, V. I., Considering Nature and Parameters of Power Suppliers for Efficient Induction Heat Treating, Industrial Heating, June 1995.

[4] Güldner, H., Hasing, C., Dierke, W., Ansteuereinrichturen lastgelöschter Wechseselrichter mit Parallelcompensation bei Verwendung integrierter Schaltkreise-Elektric, 1974, No 28, H. 6.

[5] Energetic Electronics, ed.V. A. Labuncova, Energoatomizdat, Moskow, 1987 (in Russian).

[6] Kunov, G., Velichkov, B., Bobcheva, M. Investigation of Modes of Operation of Transistor Inverter for Induction Heating, Third National Conf. Electronics'94, 28-30 Sept. 1994, pp. 49-53.

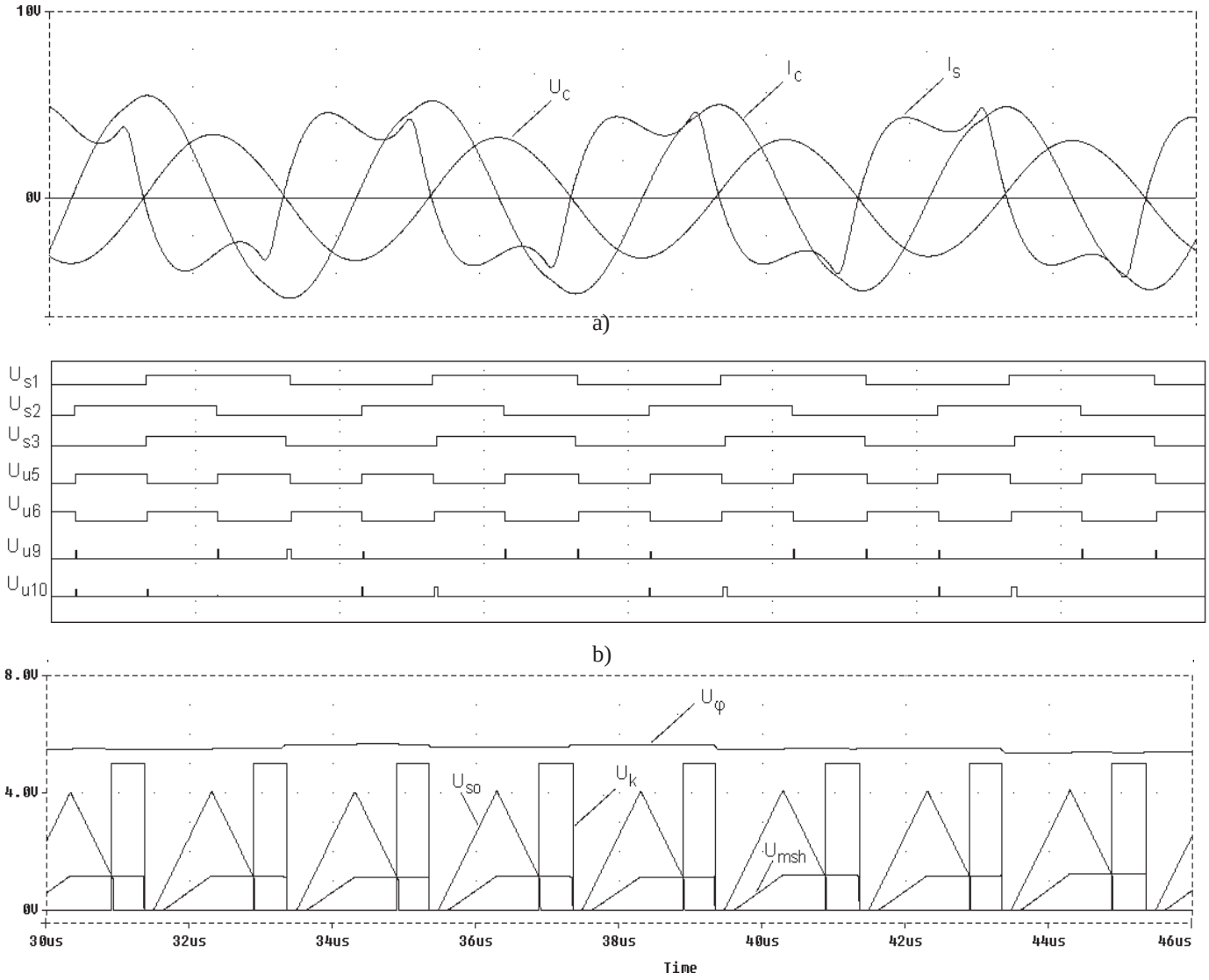

Fig. 4. Simulation results of the *PSpice* program