Improvement of Reliability of the Storage Array in Solid State Disks

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Abstract –**The causes of and the character of errors arising in the storage array are examined in the present paper. Three variants for page structure subject to processing by a correction code are discussed. A comparative analysis of the variants on the basis of several parameters is made and the most suitable for a realization has been selected.**

Key words **-Flesh memory , solid state disk**

I. TYPE OF ERRORS AND AN ANALYSIS OF THE CAUSES LEADING TO THEIR APPEARANCE IN THE STORAGE ARRAY

In 1948 Shannon [5] proved that with a proper data coding and decoding the number of errors appearing with disturbances in the channel could be reduced to the necessary minimum without any loss of information transferring speed.

Both transferring and storage of digital information have many features in common. In either case transferring of digital information is carried out from a data source to a data user. A typical system of data transferring and storage can be presented in a scheme as the one shown in fig.1.1:

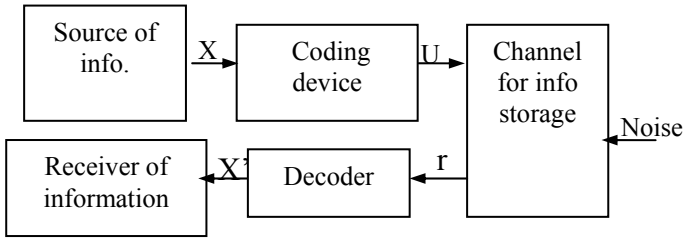

Fig. 1.1

A semi-conductor Flash memory is a medium for information storage in solid state disks (SSD). The information storage channel is generally subjected to various influences which can be of natural and man-made character such as electromagnetic disturbances, temperature change, the effect of α, β and γ particles etc.

Due to the availability of noise in the channel the accepted sequence r can not coincide with the code word U. If there is no noise in the channel, then r and X' are the copies of U and X. If the noise level in the channel is great, then X' can differ from X considerably.

The development of the coder and decoder i.e. the choice of the error detection and correction code mostly depends on the nature of the channel i.e. the type and the character of the errors that the channels introduces during data transferring.

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The main purpose of the memory is to store the information written therein in the form of binary codes with symbols 0 and 1 for a great period of time. Any random change in this information in the period between two actions of writing is called an error.

Along with the increase of the level of integration of the storage devices (SD) the number of random errors during the operation of these SD has increased. After a long period of research a conclusion has been reached that the reason for all these errors is the increased sensitivity of the SD to sunlight and radiation. This is especially valid for DRAM and Flash memory with which the principle of data storage is based on the accumulation of charges in the memory DRAM condenser and the electron accumulation in the floating gate of the cell for the Flesh memory. A Flash memory cell produced by ETOX III technology is shown in fig. 1.2.

It allows a single bit of information to be stored in each cell (1 = programmed and 0 = erased). The programming of the Flash cell is based on the mechanism of channel injection of hot electrons.

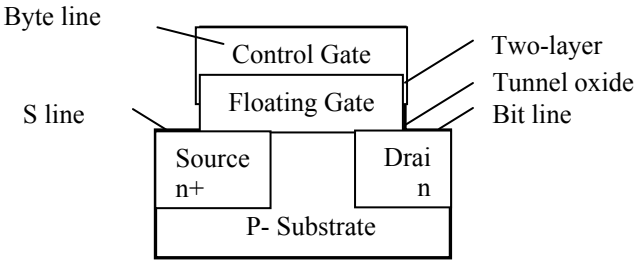
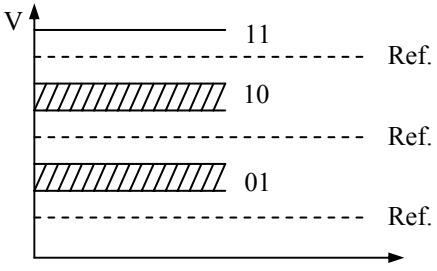


Fig. 1.2.

This way of programming is used for writing of one bit of information in one cell. The accumulation of more than 30 000 electrons in the floating gate results in a threshold level of $V_t \approx 5,5$ V i.e. write of "0". If there are fewer than 5 000 electrons in the floating gate, then "1" is written in the cell.



Фиг.1.3.

With the Intel Strata Flash technology two bytes can be written in one cell. This is possible by controlling the number of the electrons accumulated in the floating gate i.e. up to four clearly distinguished threshold voltages corresponding to the following combinations 11, 10, 01 и 00 (fig. 1.3) and corresponding to a certain Drain current for reading

respectively. It is necessary the charge to be the right dosage during programming, the levels to be accurately distinguished during reading and the charge not be leaking during information storage.

It is obvious from the research published in [6,9] that α particles while passing through silicon form a charge capable of changing the state of the storage cell. *β* и *γ* radiation do not cause such changes. The measurements of the space atmosphere and its influence on the storage element performance have established the source of *α* particles under the normal working conditions of the memory. It has proved that the material, of which the memory cases are made, contains microscopic natural admixtures of the isotopes of thorium and uranium. They are a source of *α* particles, respectively of errors. The intensity of errors is considerably increased when the memory is used at levels above sea or in the space. The greater the volume of the memory the greater the probability of a failure of any individual storage cell. [6].

The errors caused by the effects of the environment are of random character, they are single and asymmetrical. For the Flash memory made by ETOX III technology the errors are unidirectional i.e. the state of the storage cell changes from "0" to "1". For the Intel Strata Flash technology a single error can lead to one-bit or two-bit change in the stored information.

The functional operational failures lead to temporary errors that disappear after re-writing. Generally, the location of these random errors is unknown. Therefore most often the methods of correcting codes are used for correction of these errors.The usage of error correcting codes is one of the most universal methods for protection of information in the memory.

II. VARIANTS FOR STRUCTURE OF CORRECTING CODES AND ANALYTICAL CALCULATION OF THEIR MAIN PARAMETERS

While selecting the type of the correcting code and the schematic solution of the coder and decoder the design features of the Flash memory being the basic element of the storage array should be taken into consideration. The main requirements are as follows:

- the time for access to the stored information should not be increased
- the code selected should ensure a high degree of error detection and detection
- the coefficient of information redundancy *R=r/k* as well as the hardware redundancy should be low because they also can be a source of errors

With the universal application memory the access to any cell is random whereas with the storage array memory there is page structuring. The operation write or read is effected over a page including 256 words of 16 bits each. The information redundancy for the block dividable codes can be formed by increasing the bits for the words - (*16+r)* bits i.e. by vertical control or by increasing the number of the 16-bit (*256+r*) i.e. by horizontal control (fig. 2.1).

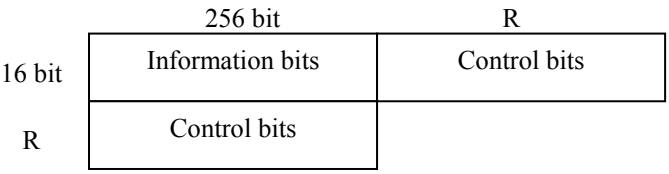


Fig. 2.1

When using the Strata Flash technology the errors are independent and symmetrical. However, an error in one storage cell may lead to a change of one or two bits. If two bits are changed, then they are certain to be located in the word (16 bit) in which the storage cell is included.

A. A variant for information coding and correction by words

In this variant (fig. 2.2) each word written in the sector is coded and *r* control bits are added to it.

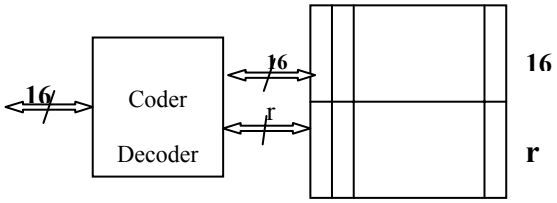


Fig.2.2

When selecting a correction code with this variant due regard should be given to the fact that a single error in the storage cell can result in an equally probable single or double error in the bits. That's why it is obligatory to select a code capable of correcting double errors. The most suitable code for this case is the BCH code named after its founders – mathematicians. [6].

At coding distance *d=5* the code will detect and correct a single and double error. At coding distance *d=6* the code will correct a single and double error and will detect a triple error. The total length of bits at *d=6* is calculated by the formula:

$$n = 2^{(r-1)/2}, \qquad (2.1)$$

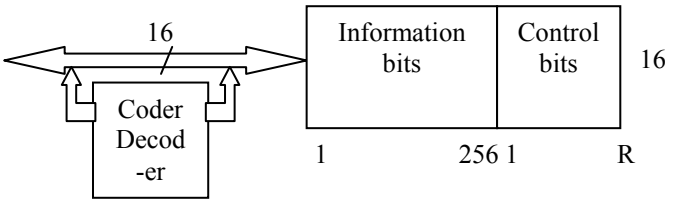
where *r* is an odd number. With byte structure shortened codes are used. With 16 information bits *r* is equal to 11, and the total number of bits is equal to 27 [6]. The information redundancy is equal to:

$$R = \frac{r}{n} = \frac{11}{27} \approx 0{,}4 \qquad (2.2)$$

This is a very high coefficient of information redundancy. It can be considered that BCH code will not decrease the total transfer rate.

B. A Variant for horizontal control

With this variant bits under the same number of each word of the page are subject to control. The length of the entire block will be equal to *n=256+r* bits. Coding and decoding will be effected simultaneously by 16 identical schemes (fig. 2.3) - one for each bit position of the array.



Фиг.2.3.

An error arising in one storage cell of the memory can lead to a single error in the code word. The most suitable code for this case is the cyclic code of Hamming. At code distance *d=3* the code of Hamming detects and corrects single errors, at *d=4* the code corrects single and detects double errors [6,9]. At code distance *d=3* the length of the code word is $n=2^r-1$, and of the information bits is $k=2^m-m-1$. At code distance *d=4* the number of the control bits is increased by 1. When using blocks with byte structure shortened codes of Hamming are used and for $\kappa=256$ according to [5] the number of the control bits is *r=10*. The code of Hamming for *d=4* is of the type (266, 256). The information redundancy is equal to:

$$R = \frac{r}{n} = \frac{10}{266} \approx 0{,}038 \qquad (2.3)$$

This is a relatively low coefficient for information redundancy.

This variant causes changes in the transfer rate for operations write and read. Instead of 256 cycles the sector will be transferred for 266 cycles by the data bus. This reduces the transfer rate with about 4 %.

Also, the access time to the information during "read" operation will increase. When using the code of Hamming it is obligatory for the entire sector to be written in the memory before the start of "read" along with the simultaneous error correction. This causes a delay of the information for a period which is calculated by the formula:

$$t_з = 266.t_ц = 266.50ns = 13{,}3\mu s \qquad (2.4)$$

C. A variant of horizontal control - modified

with this variant the control is horizontal as in item 2.2 but the length of the information bits is 64 (fig.2.4).

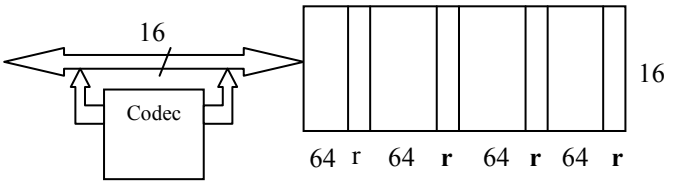


Fig.2.4.

The decrease of the length of the information block has several aims:

- to increase the average time between two failures
- to decrease the time for access to the information
- to locate the incorrigible error more accurately

In this case a single error in the storage cell will cause error in the code word. With the code of Hamming at code distance *d=4* and using of shortened code, the number of the control bits is *r=8*. The code of Hamming is of the type (72, 64). The information redundancy is equal to:

$$R = \frac{r}{n} = \frac{8}{72} \approx 0{,}011 \qquad (2.5)$$

The time necessary to transfer data to a block in FIFO and its correction will be equal to:

$$t_з = 72.t_ц = 72.50ns = 3{,}6\mu s \qquad (2.6)$$

The transfer rate for reading a sector will also decrease. 288 cycles will be necessary for reading one sector instead of 256 cycles i.e. the transfer rate will drop with about 13 %.

D. A comparative analysis of the parameters of variants 1, 2 and 3

The probability of one error arising in *n* bits can be calculated by the following formula:

$$P_n(l) = C_n^l.q^l.(1-q)^{n-l}, \qquad (2.7)$$

C_n^l is a combination of *n* elements l^{th} class, and *q* is the probability for the appearing of one error. With *n* greater than 10 and with $q<<1$ formula (2.7) will be of the type:

$$P_n(l) = \frac{(q.n)^l}{l!}.e^{-q.n}$$

The possibilities for error detection and correction depend on the code distance of the code selected. With variant 1 the code distance is *d=6* (fig. 2.5).

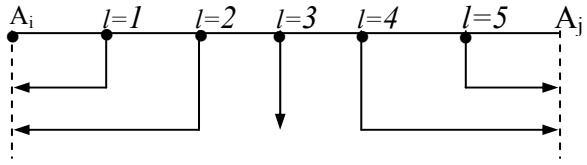


Fig. 2.5.

With this variant the probability for data correctly read P_n, the probability for detection of incorrigible error $P_{нк}$ and the probability for transformation in a wrong code word P_m are given below:

$$\begin{cases} P_{П}(27) = P_{27}(0) + P_{27}(1) + P_{27}(2) \\ P_{НК}(27) = P_{27}(3) \\ P_T(27) = P_{27}(4) + P_{27}(5) + P_{27}(6) + \ldots \end{cases} \qquad (2.8)$$

With variant 2 and 3 the code distance is *d=4* (fig.2.6)

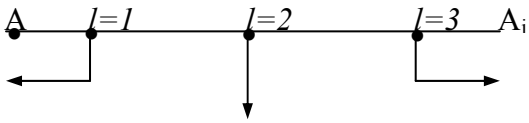


Fig. 2.6

The probabilities P_n, $P_{нк}$ and P_m for *n=72* and *n=266* respectively are given below:

$$\begin{cases} P_{\Pi}(72) = P_n(0) + P_n(1) \\ P_{HK}(72) = P_n(2) \\ P_T(72) = P_n(3) + P_n(4) \end{cases} \quad (2.9)$$

When calculating these probabilities the selection of the parameter q namely, the probability for a single error in the storage cell, is of paramount importance. There are no concrete values for the parameter q in literature that is why the probabilities P_n, $P_{нк}$ and P_m will be calculated for one and the same values for q. With variant 1 when selecting q it has been taken into account that a single error in the storage cell causes a single or double error in the bits, the probability being equal. The results of the calculations are given in fig.2.7 and fig. 2.8.

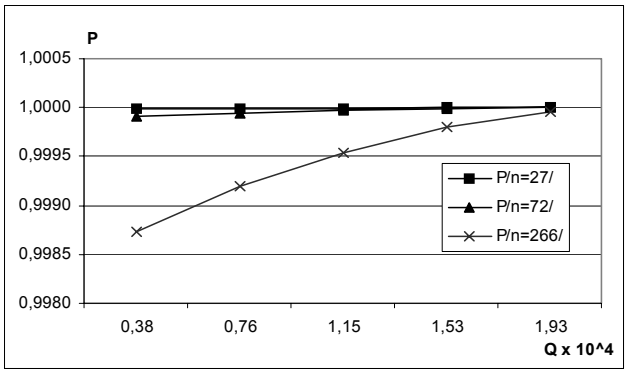


Fig. 2.7

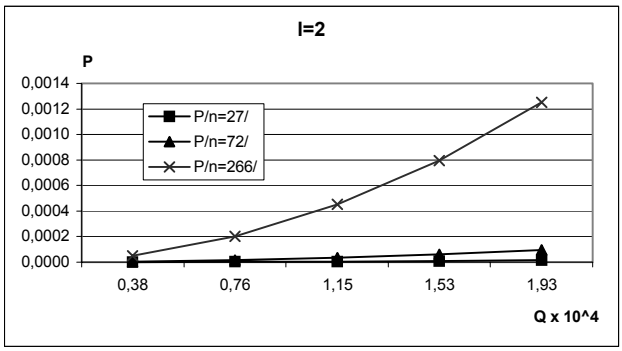


Fig. 2.8

On the basis of the analysis of the results a conclusion can be drawn that variant 1 followed by variants 3 and 2 has the highest degree of probability for error detection and correction. With the increase of n, probabilities $P(l)$ decrease.

The second main parameter characterizing the corrective properties of the codes selected is the average time for failures i.e. the average time between two failures which can be detected but not corrected. For the code of Hamming with the code distance of $d=4$ (variant 2 and 3) this is the double error. The average time between two failures for this variant is calculated by the formula (2.10) [7].

$$T_{cp.} = \frac{T_k}{C} \cdot \frac{k}{n} \cdot \sqrt{\frac{\pi}{2} \cdot \frac{C}{k}}, \quad (2.10)$$

where $T_к$ is the average time between two errors in one cell (bit) of the memory;

C –information volume of the memory in the disk;
n – total length of the code word (27, 72, 266);
k – information bits in the code word (16, 64, 256).

The value of $T_к$ is in the order of 10^{10}-10^{11} [1] and these values are for memory produced in 1985. The memory that we have used namely, Flash memory will be produced by the Strata Flash technology but no data for the parameter $T_к$ are available in the literature. However, it is for sure that the values of this parameter are better than the values obtained through the technologies used in the middle of the 80-ies. The change of $T_{cp}=f(S, Tk, k, n)$ for the values of $T_к = 5.10^{10}$ are clearly obvious in the graphics in fig. 2.9.

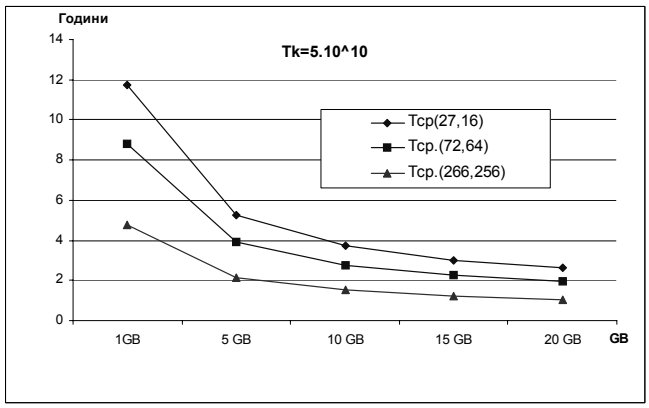


Fig. 2.9

The following conclusions can be drawn:

- For one and the same values of $T_к$ and C variant 1, followed by variants 3 and 2, has the greatest time between two failures.
- With the increase of the disk capacity, $T_{cp.}$ decreases.
- The relation between $T_к$ и $T_{cp.}$ is directly proportional. With the improvement of technology and increase of $T_к$ the total reliability of the disk will improve
- Variant 3 is a quite reasonable solution. It is this variant for memory structure and error detection and correction code that will be realized.
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